%signals HH DORSHHHTVVVORSHHH

%signals 12 GGGW321G321GGW321

%signals .BBBBBB.CCCAAAAAA

H3A = 00000000000000000000000000001

H2A = 00000000000000000000000000010

H1A = 00000000000000000000000000100

SWA = 00000000000000000000000001000

RGA = 00000000000000000000000010000

OGA = 00000000000000000000000100000

V1 = 00000000000000000000001000000

V2 = 00000000000000000000010000000

V3 = 00000000000000000000100000000

TG = 00000000000000000001000000000

H3B = 00000000000000000010000000000

H2B = 00000000000000000100000000000

H1B = 00000000000000001000000000000

SWB = 00000000000000010000000000000

RGB = 00000000000000100000000000000

OGB = 00000000000001000000000000000

DG = 00000000000010000000000000000

HD1 = 00001000000000000000000000000

HD2 = 00010000000000000000000000000

%here we define status of clocks

%Mapping skipper clocks to LTA

%Horizontal clocks

%H1A = H1U

%H3A = H3U

%H1B = H1L

%H3B = H3L

%H2A y H2B=H2

STATE_3DG = OGB | RGB | SWB | H1B | TG | V3 | V1 | OGA | RGA | SWA | H3A

STATE_4 = DG | OGB | RGB | H2B | H1B | TG | V3 | V1 | OGA | RGA | H3A | H2A

STATE_5 = DG | OGB | RGB | H2B | TG | V3 | V1 | OGA | RGA | H2A

STATE_6 = DG | OGB | RGB | H3B | H2B | TG | V3 | V1 | OGA | RGA | H2A | H1A

STATE_7 = DG | OGB | RGB | H3B | TG | V3 | V1 | OGA | RGA | H1A

STATE_8 = DG | OGB | RGB | H3B | H1B | TG | V3 | V1 | OGA | RGA | H3A | H1A

STATE_9 = DG | OGB | RGB | SWB | H3B | H1B | TG | V3 | V1 | OGA | RGA | SWA | H3A | H1A

STATE_10 = DG | OGB | RGB | H3B | H1B | TG | V3 | V1 | OGA | RGA | H3A | H1A

STATE_10RG= DG | OGB | H3B | H1B | TG | V3 | V1 | OGA | H3A | H1A

STATE_10RB= DG | H3B | H1B | TG | V3 | V1 | H3A | H1A

%Vertical clocks

STATE_11= DG | SWB | H3B | H1B | V3 | V1 | SWA | H3A | H1A

STATE_12= DG | SWB | H3B | H1B | V1 | SWA | H3A | H1A

STATE_13= DG | SWB | H3B | H1B | V2 | V1 | SWA | H3A | H1A

STATE_14= DG | SWB | H3B | H1B | V2 | SWA | H3A | H1A

STATE_15= DG | SWB | H3B | H1B | V3 | V2 | SWA | H3A | H1A

STATE_16= DG | SWB | H3B | H1B | TG | V3 | SWA | H3A | H1A

%%States for CDS

%Pedestal CDS

STATE_8B= HD1 | DG | OGB | RGB | H3B | H1B | TG | V3 | V1 | OGA | RGA | H3A | H1A

STATE_8C= DG | OGB | RGB | H3B | H1B | TG | V3 | V1 | OGA | RGA | H3A | H1A

%Signal CDS

STATE_10A= HD2 | DG | OGB | RGB | H3B | H1B | TG | V3 | V1 | OGA | RGA | H3A | H1A

STATE_10B= DG | OGB | RGB | SWB | H3B | H1B | TG | V3 | V1 | OGA | RGA | SWA | H3A | H1A

%MODEL = HD2 | HD1 | DG | OGB | RGB | SWB | H3B | H2B | H1B | TG | V3 | V2 | V1 | OGA | RGA | SWA | H3A | H2A | H1A

%here we define loop variables

%Small Skipper

NROW = 700

NCOL = 400

```
%Large 4k Skipper
%NROW        = 2200
%NCOL        = 500

NSAMP       = 1  % SKIPPER SAMPLES
%robin          = 0  %BINNING FACTOR FOR ROWS


%Dummy variable for fits header: Physical parameters of the CCD
CCDNPRES=  7

%Small Skipper
CCDNROW = 1248
CCDNCOL = 724

%Large 4k Skipper
%CCDNROW = 4126
%CCDNCOL = 886

%here we define delay variables
delay_H_overlap       = 100                % Time between phases of Horizontal clock
delay_Integ_Width     = 1200               % Integration time
delay_PedIInteg_after = 30

delay_SWhigh          = 50
delay_SW_after        = 30
```

```
delay_H_after        = 10

delay_og_low     = 100                % Time during OG and SW down. Charge going back into the SW from the SN

delay_V_Overlap       = 1000                % Time between phases of Vertical clock

delay_RG_Width = 100

delay_RG_after =30


%here is the program

delay CCDNPRES   %Just for the variable to appear en header

delay CCDNROW    %Just for the variable to appear en header

delay CCDNCOL    %Just for the variable to appear en header

%

loop NROW

        %

        loop NCOL

                %

                status STATE_3DG

                delay delay_H_overlap

                status STATE_4

                delay delay_H_overlap

                status STATE_5

                delay delay_H_overlap

                status STATE_6

                delay delay_H_overlap

                status STATE_7

                delay delay_H_overlap

                status STATE_8

                delay delay_H_overlap

              %SKIPPER%-----------------------------------------------------------------
```

```
status STATE_10RG
  delay delay_RG_Width
    %
    loop  NSAMP      % BEGIN Loop SKIPPER SAMPLES
          status STATE_8
          delay delay_RG_after
       %START OF PEDESTAL INTEGRATION%-------------------------------------
          status STATE_8B
          delay delay_Integ_Width
          %status STATE_8C
          %delay delay_PedlInteg_after
          status STATE_9
          delay delay_SWhigh
          %status STATE_10
          %delay delay_SW_after
          %END OF PEDESTAL INTEGRATION%-----------------------------------------
--
       %
          %START OF SIGNAL INTEGRATION%-----------------------------------------
-
          status STATE_10A
          delay delay_Integ_Width
          %status STATE_10B
          %delay delay_H_after
       %END OF SIGNAL INTEGRATION%-------------------------------------------
       %
          status STATE_10RB
          delay delay_og_low
          status STATE_10RG
```

```
                delay delay_RG_Width
            endsync
            %
            status STATE_9
            delay delay_SWhigh
            %status STATE_8
          %delay delay_H_after
            %
      endsync
      %
          status STATE_11
        delay delay_V_Overlap
            status STATE_12          %V3 -> LOW
            delay delay_V_Overlap
            status STATE_13          %V2 -> HIGH
            delay delay_V_Overlap
            status STATE_14          %V2 -> LOW
            delay delay_V_Overlap
            status STATE_15          %V3 -> HIGH
            delay delay_V_Overlap
          %
          status STATE_16             %V2 -> LOW; Tg -> HIGH
        delay delay_V_Overlap
endsync
```