Low Threshold Acquisition Controller for Skipper Charge Coupled Devices

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***Abstract*—In this work, the design and preliminary results of the first specially design Skipper-CCD controller, aimed for low threshold particle and astronomy experiments, is presented. The system integrates on a single board: the generation of the clock and bias signals for the sensor; four high-speed analog-to-digital converters to digitize the video channels of the CCD; Artix-7 FPGA to perform pixel calculation and board control; a front panel connector for all the signal inspection; and Ethernet port for full operation and data collection through standard network connection to a PC. The system has been fully tested and sample images were taken for both conventional and Skipper-CCDs.**

***Index Terms*—CCD controller,fully-depleted CCD, skipper CCD, First Controller Skipper CCD.**

I. Introduction

Initially presented as memory solutions [1], [2], Charge Coupled Devices (CCDs) have found a niche as imaging detectors due to their ability to obtain high resolution digital images. In particular, scientific CCDs have been extensively used in ground and space-based astronomy and X-ray imaging [3]. CCDs have low read-out noise, good spatial resolution, and low dark current. Furthermore, CCDs can be made thick and fully-depleted to increase its detection mass, enabling their use as particle detectors [4]. The low read-out noise can be as low as $2\,\mathrm{e}^-$, which enables obtaining a low energy threshold of 5.5 eV. Recently, with the development of fully-depleted Skipper-CCD, it has been possible to achieve a extremely low readout noise of $0.068\mathrm{e}^-$ [5], [6]. Currently, the Sub-Electron-Noise Skipper-CCD Experimental Instrument (SENSEI) will use $\sim$50 skipper-CCD to achieve a 100 gram mass for dark matter searches[7]. Other experiments like CONNIE (Coherent Neutrino-Nucleous Interaction Experiment)[8] and DAMIC (Dark Matter in CCDs)[9] are planning to migrate to this new skipper-CCD technology. This context has motivated the development of a low-noise electronic controller for Skipper-CCD, which will ease the migration for the mentioned experiments. The design of the so called Low-Threshold Acquisition (LTA) system is presented in Section II. Experimental results obtained with Skipper-CCD are shown in Section III, and Section IV summarizes and concludes the work.

II. System design

The system is integrated into an easy to use single PCB board. Compared to other readout systems for CCD-based detectors [10], it uses a single $12\,\mathrm{V}$ power supply and an Ethernet connection. The block diagram of the readout system is shown in Fig. 1.

The data processing and control of the peripheral components is done by the Artix-7 FPGA. Bias voltage together with clock generation units create the signals that are necessary to drive the CCD, which integrates four output video channels. The video channels are digitized using four 18-bit, 15 MSPS analog-to-digital converters. A detailed description of the design and test of the front-end electronics can be found in [11]. The user interacts with the board through a single Ethernet port, which allows sending and receiving commands as well as data. Serial interface is reserved for debugging purposes.

The clock generation unit is able to create the control signals that allow moving the charge in the CCD to drive the output video amplifiers. These signals require precise timing control, and also varying voltages for low and high states. Using high voltage-swing digital-to-analog converter, fine tuning of these voltages is possible. The sequencer integrated into the FPGA creates the timing signals that switch the low and high values of the clocks.

Various bias voltages are required to polarize not only the internal video amplifiers of the CCD, but also some extra active components that are close to it for signal conditioning purposes. These voltages are all generated using a combination of switching converters, LDOs and digitally controlled resistors. This combination allows the user to configure the value of the particular bias voltage on the fly from the remote Ethernet connection. Voltage sources and the related switching frequencies must be carefully chosen to minimize overall noise of the system.

One of the main and most critical components of the CCD-readout system is the high-speed video acquisition. To achieve ultra-low readout noise figures, it is indispensable to minimize electronic noise sources that couple in the video signal. The video signal path was carefully designed to minimize such

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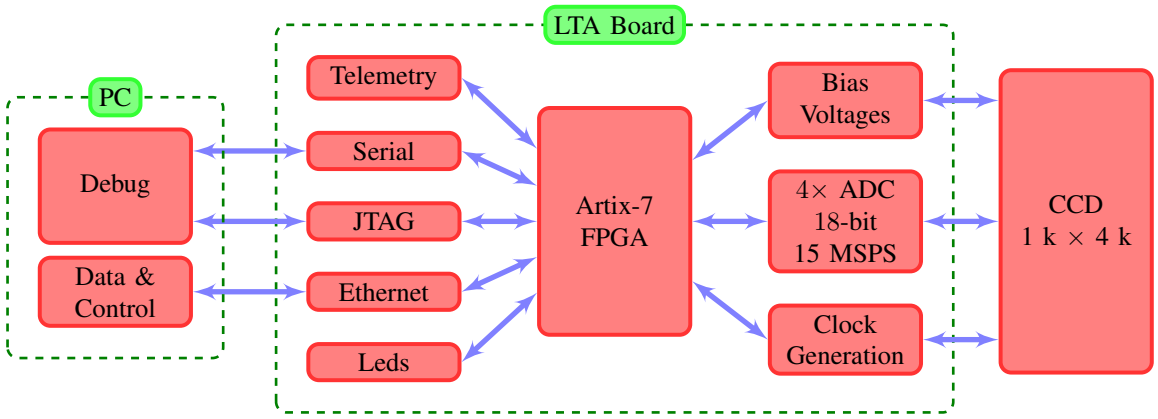

Fig. 1: Block diagram of the readout system detailing the connectivity between the control LTA board, the computer and the CCD sensor.

interactions, with the overall electronic noise of the video signal being dominated by the intrinsic noise of the CCD chip. The board has four video channels, built with 18-bit, 15 MSPS analog-to-digital converters tightly coupled with low-noise differential operational amplifiers. Output samples of the converters are fed into the FPGA to perform digital filtering and image reconstruction. Output data is sent through the Ethernet port. All four channels are read simultaneously, minimizing the total read time of the CCD.

Experiments targeted for using the described system tend to be remotely controlled. In most cases, the readout system is not accessible by the user as it can be installed in remote places like deep underground or in high radioactive spaces. As a result, it is extremely important for the end user to be able to monitor key variables of the system remotely. The readout board incorporates a low-speed analog-to-digital converter together with analog multiplexers, that allow monitoring all voltages and clock signals. This sub-system is called telemetry, and the data collected can be transferred using the Ethernet port. In this way the user can monitor the internal variables of the system remotely, without the necessity of adding extra hardware or complex communication mechanisms.

The control of the board as well as video processing is performed by the Artix-7 FPGA. JTAG port connectivity was added to easy programming and debugging. Non-volatile 512 MB flash memory is also added to allow the board to store the FPGA bit-stream for permanent, non-JTAG functioning. A block diagram of the capabilities included on the FPGA firmware are depicted in Fig. 2.

Most of the capabilities of the board are added as custom AXI peripherals, as it is shown in the figure. A low complexity soft-microblaze processor is included as part of the FPGA firmware to control these peripherals. Low-level drivers were developed to control the blocks through simple system calls. In this way the user can send commands to the board through the Ethernet port, and the processor will configure the peripheral. The video path starts in the $4\times$-video inputs, that are digitized and sent to the FPGA using high-speed LVDS

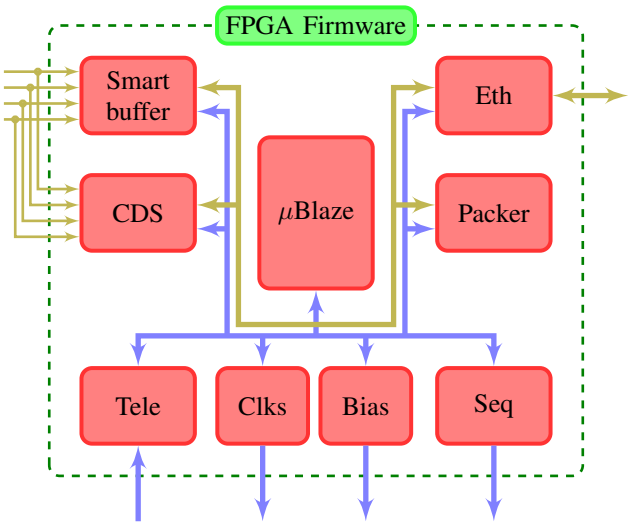

Fig. 2: Detail of the FPGA firmware with low-speed control AXI bus (—) and high throughput data paths (—).

serial interfaces. The FPGA includes high-speed transceivers that allow capturing the data avoiding common timing issues. Digital samples of the four video channels are routed into the so called Correlated Double Sampling (CDS) block and the smart buffer. Outputs of these two blocks inject the resulting data into the Ethernet unit, which includes a high-speed burst input for continuous data transfer.

One important feature of the system that can be used to better understand the source of noise is having access to the raw video signal. During the readout process, the video signal is sampled at 15 MSPS using 18-bit resolution. Standard CCD chips used for high-energy physics applications have a resolution of 4000×1000 pixels, with a pixel duration that varies between $30 - 100\,\mu$s. The resulting digital data stream can have $450 - 1500$ samples per pixel. With these numbers, a full image can have as much as 6 G samples, which represents $\approx$ 14 GB of information. It should be clear that it is not easy to store a full image on the FPGA's internal memory

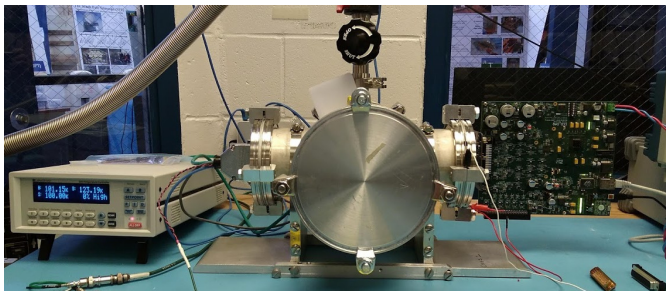

Fig. 3: Photograph of the experimental setup. Includes temperature controller, dewar and LTA electronics.

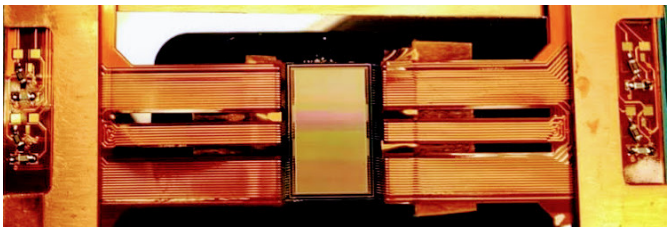

Fig. 4: Picture of the Skipper-CCD that is inside the dewar of figure 3.

for further analysis. Due to the speed of the data stream, it is not possible to transfer raw data on real time. As a result of these limitations, the system includes a Smart Buffer to store raw data on a controlled manner. This block was developed to behave like an integrated oscilloscope, which means the user can configure it to capture one, two or the four raw video channels. Single or continue capture is also supported. As an extra feature, signals from the sequencer are routed to the buffer and are used like external triggering, allowing to store data samples at very precise moments. Data stored by the Smart Buffer is kept until the user decides to transfer it using the Ethernet interface using a lower speed which can also configured on the fly. This tool was proven to be useful in the process of understanding the sources of noise present on the video signal.

III. Results and Measurements

The LTA board was used to read an image from a Skipper-CCD. The experimental setup used for the test can be seen in Fig. 3. A photograph of the 1248×724 pixels CCD is shown in Fig. 4. The CCD is located inside a thick Aluminum box (Dewar) at high vacuum and at a temperature of 110 k. The CCD has four quadrants each of which has a readout amplifier. An image of a fraction of the CCD is shown in Fig. 5. Events such as electrons, muons and X-rays can be observed in this photo. Those events were obtained with an overnight exposure of more than seven hours. The CCD is exposed to a ^{55}Fe X-ray source (5.9keV) through a small opening in the cover of the detector. The bright white area corresponds to many X-ray events overlapping each other. Some additional single-pixel X-ray events can be appreciated above this region, this events are capture during the readout process when the rows

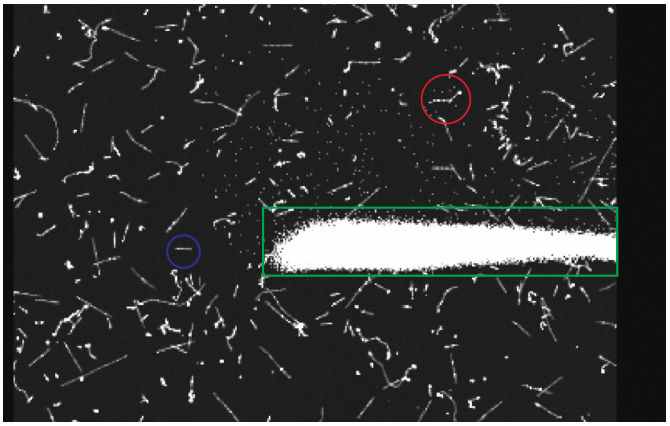

Fig. 5: Image taken with the readout system. Highlighted with a red circle is an event produced by an electron, in blue by a muon, and inside a green box are events generated by a X-ray source

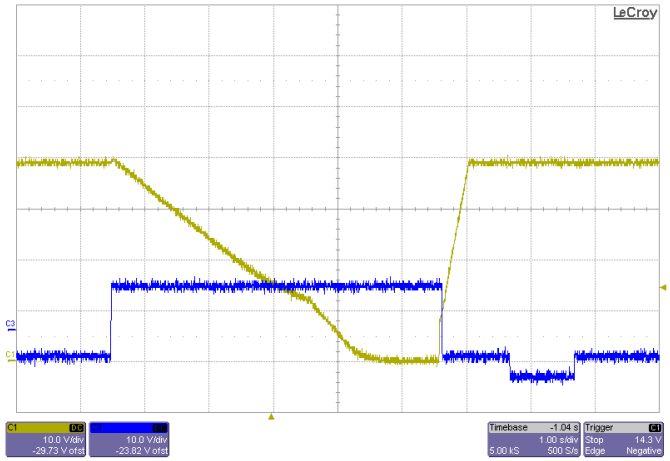

Fig. 6: Erase procedure. Channel-1 (curve in yellow) shows the substrate voltage going from 40 V to 0 V and back to 40 V and one of the vertical clocks going to 9 V and back to normal operation voltage.

of the CCD are being shifted. Other events, such as straight lines correspond to atmospheric muons crossing the detector and the worm-shaped events are produced by high energy electrons coming more likely from Compton interactions of natural radioactivity photons. The black region at the right of the image is referred to as overscan, and corresponds to extra columns of empty pixels [3].

A. Erase and E-purge procedures

As reported in [12], [4], when CCDs are first turned on, or when they are saturated because they have been exposed to strong illumination, residual "ghost" images or high dark current signals are produced. Dark current is the reverse bias leakage current in non-imaging devices. At low temperatures, the process of "cleaning" the CCD to remove the excess charge, through repetitive reading can extend over many hours.

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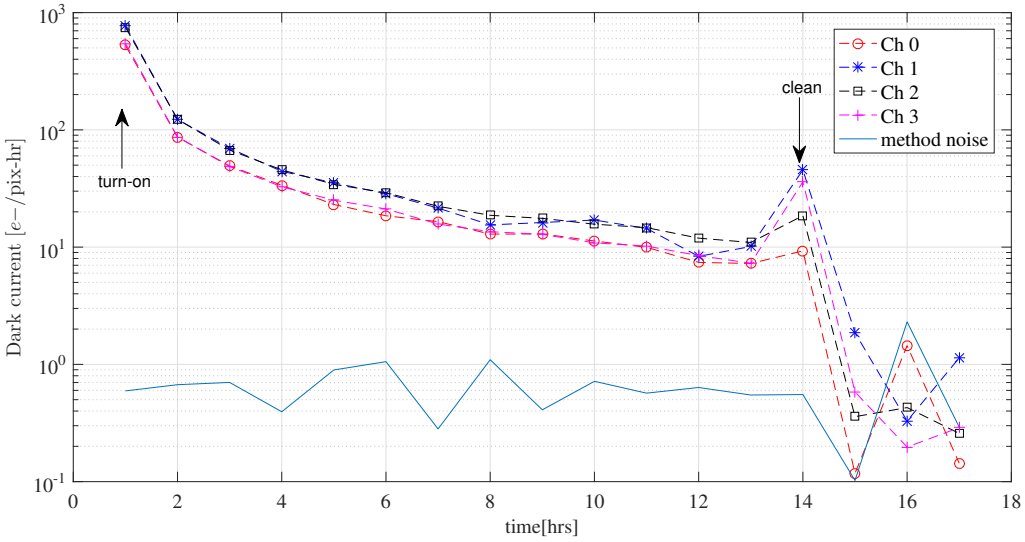

Fig. 7: Dark current as a function of time. At time $t = 1$ the CCD is turned on an read every hour. At $t = 14$ the clean procedure is performed. The solid line indicates the limiting noise for the dark current computation method.

Instead, dark current can be dramatically reduced by the erase procedure reported in [4]. This method was implemented in the LTA: the CCD substrate bias voltage is lowered to 0 V (with a controlled slope) and all vertical clocks are increased to their higher level. The oscilloscope capture for the substrate voltage going from 40 V to 0 V and back to 40 V is shown in Fig. 6. To allow fine control of the timing and required slope, this functionality was added as a monolithic function that is executed from the integrated microprocessor in the board. The user sends a specific command to the board to execute the procedure through the Ethernet connection.

After performing the erase procedure, all the parallel clocks are set to a -9 V, and hold at this voltage for a fraction of a second before restoring normal operation, this procedure is known as e-purge [12]. Finally a fast readout of the CCD is done to complete the cleaning procedure which takes less than one minute.

The aforementioned CCD cleaning method was tested to demonstrate the decrease in dark current, and experimental results are shown in Fig. 7. The power of the CCD is switched on and one image is taken every hour. The difference between the median of the charge of 625 pixels in the active region of the detector and the median of the same amount of pixels in the overscan region (free of charge) is computed. This difference of charge is caused by dark current which affects the active region. Figure 7 shows the result of the four readout channels of the CCD. It also shows the difference between two different overscan regions of the image to give an idea of the limitation of the method used to compute the dark current. The measurement presented in Fig. 7 is only corrupted by the readout noise and, since to compute the curves several pixels of the CCD are averaged, this noise contribution is reduced significantly on each measurement.

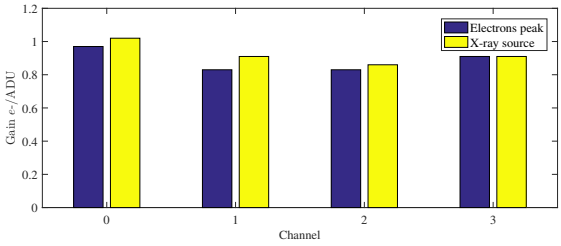

Fig. 8: Gain calibration using ^{55}Fe X-ray source and single-electron detection capabilities of Skipper-CCD.

The curve labeled as "method noise" is computed as the absolute value of the difference between the median of two empty regions of the CCD. Since this region have no charge a zero value is expected, this curve is an indication of the expected measurement error.

The erase, e-purge and readout procedures to clean out the CDD are executed at $t = 14$. As it can be clearly seen, the dark current is reduced by one order of magnitude to the error levels of the measurement technique. It only takes less than one minute to perform the cleaning procedure, in comparisons to cleaning the CCD by several readouts (from time $t = 2$ to $t = 12$).

B. LTA current performance

1) Gain calibration: In CCDs readout systems it is common practice to compute the noise of the system in units of electrons RMS [3]. It is necessary to evaluate the gain of the complete system between the sense node (SN) capacitance and the analog to digital converter units: $\mathrm{e}^-/\mathrm{ADU}$. If the sensitivity $\mu\mathrm{V}/\mathrm{e}^-$ of the SN, the gain of the amplifiers stages, and the ADU-Volts relation of the AD converter are precisely

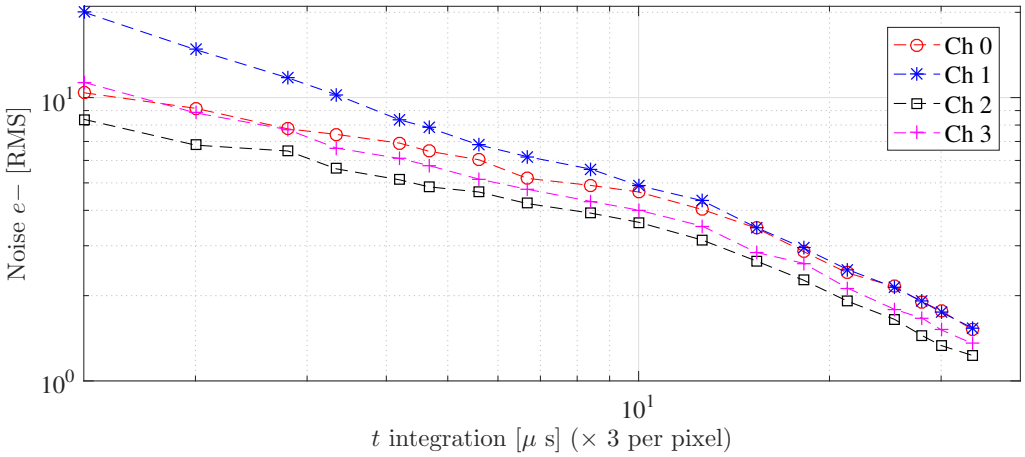

Fig. 9: Noise measured in electrons as a function of the integration time. Three integration intervals are used in each pixel.

known, this gain can be computed analytically [11]. However, it is usually preferred to evaluate the gain using other methods. One method is based on exposing the CCD to 5.9 keV X-ray from the ^{55}Fe source. After taking an image and computing the events histogram a peak can be observed that correspond to the average electron-holes pairs generated by the X-ray source in silicon, using the conversion factor of $3.77\,\mathrm{eV/e^-}$ the gain for all the channels can be obtained. In the case of Skipper-CCD it is also possible to take several measurement of the same pixel charge, then to average the results and reduce the noise at the point in which single electrons events can be detected and used to compute the gain (see Section III-C). A comparison of the gain obtained by both methods can be seen in Fig. 8.

2) Noise scan: The noise performance of the readout system was evaluated for different pixel integration times. The setup shown in Fig. 3 was used with a Skipper-CCD that has 4 readout channels. The read out techniques uses a novel digital algorithm to reduce the correlated noise of the channels by using optimal weights to subtract the noise of each channel using information of the noise in two other channels. This method has been recently developed by the authors and will be the subject of another work. The algorithm requires three integration intervals per pixel compared to the standard correlated double sampling method that requires two integration intervals. The readout noise of the system with the proposed method can be appreciated in Fig. 9. As an example, for an integration time of $12.6\,\mu$s, the noise in channel 2 is $3.14\,\mathrm{e^-}$. Differences among the channels are due to different design of the output stages of the CCD.

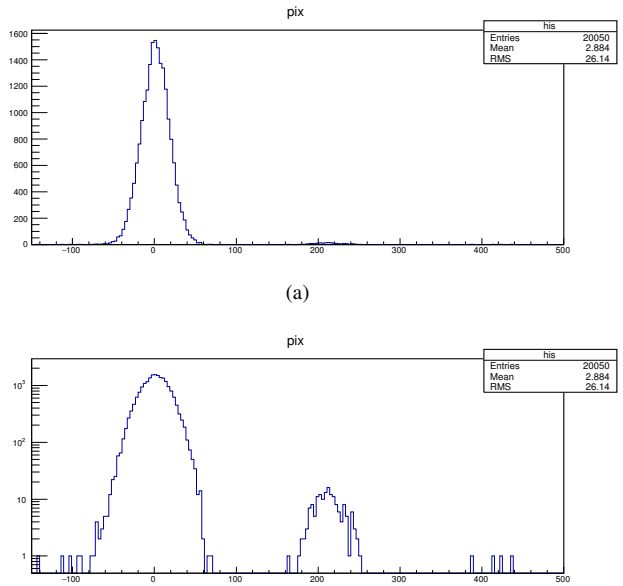

Fig. 10: Histogram computed for the pixels of a Skipper-CCD image. x-axis: analog to digital converter units (ADU); y-axis: amount of pixels.

C. Skipper-CCD image

An Skipper-CCD image reading out 2000 times the charge of each pixel was taken from a fraction of the CCD of size 50×401 pixels. To compute each pixel, three intervals of $\mathrm{N} = 189$ ADC samples are digitally integrated by the correlated double sampling (CDS) in the FPGA. Figure 10 shows a histogram

of the pixels for channel-3 after averaging the 2000 readouts of each pixel, Fig. 10a shows the y-axis in linear scale while Fig. 10b shows the result with the y-axis in log scale. Two peaks with Gaussian distribution can be appreciated. This two peaks correspond to empty pixels (highest peak) and pixels with single electrons events (lowest peak). This histogram can be used to determine the $\mathrm{e}^-/\mathrm{ADU}$ gain of the system, since the difference between the location of the two peak centers correspond to one electron. The standard deviation (STD) of the Gaussian distributions gives the noise of the system. Since the CDS computes the sum of the samples without dividing by N, the gain of the system can be computed after fitting the mean μ and STD σ of the two peaks as

$$G = \frac{1e^- \times N}{(\mu_1 - \mu_0)} = \frac{1e^- \times 189}{(210.5 - 1.2)} \approx 0.9e^-/\mathrm{ADU}. \quad (1)$$

where μ_0 and μ_1 are the means. The noise for this channel is

$$\text{noise} = \frac{\sigma}{N} G = (16/189)0.9 \approx 0.076e^-. \quad (2)$$

This noise has the expected value, since from Fig. 9 the noise for a single-time read out of the charge per pixel for $\mathrm{T_s} = 12.6\,\mu\mathrm{s}$ for channel-3 is $3.5\,e^-$ and after 2000 read outs of each pixel charge, it is expected to reduce the noise by the square root [7]: $3.5/\sqrt{2000} \approx 0.076\,\mathrm{e}^-$.

IV. Conclusion

In this work the first CCD controller specially designed for Skipper-CCD was presented. This type of CCD allows to readout nondestructively the same pixel charge multiple times, which reduces the readout noise. To drive skipper-type CCDs it is necessary to have the flexibility of sequencing the clocks in a different way compared to standard CCDs. The controller is a fully digital, single board, 4-channels, Ethernet based system which provides the necessary signals and sequencing flexibility. A detailed description of the main components and functionalities of the system were presented. The results from standard tests for CCD were detailed to show its performance.

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