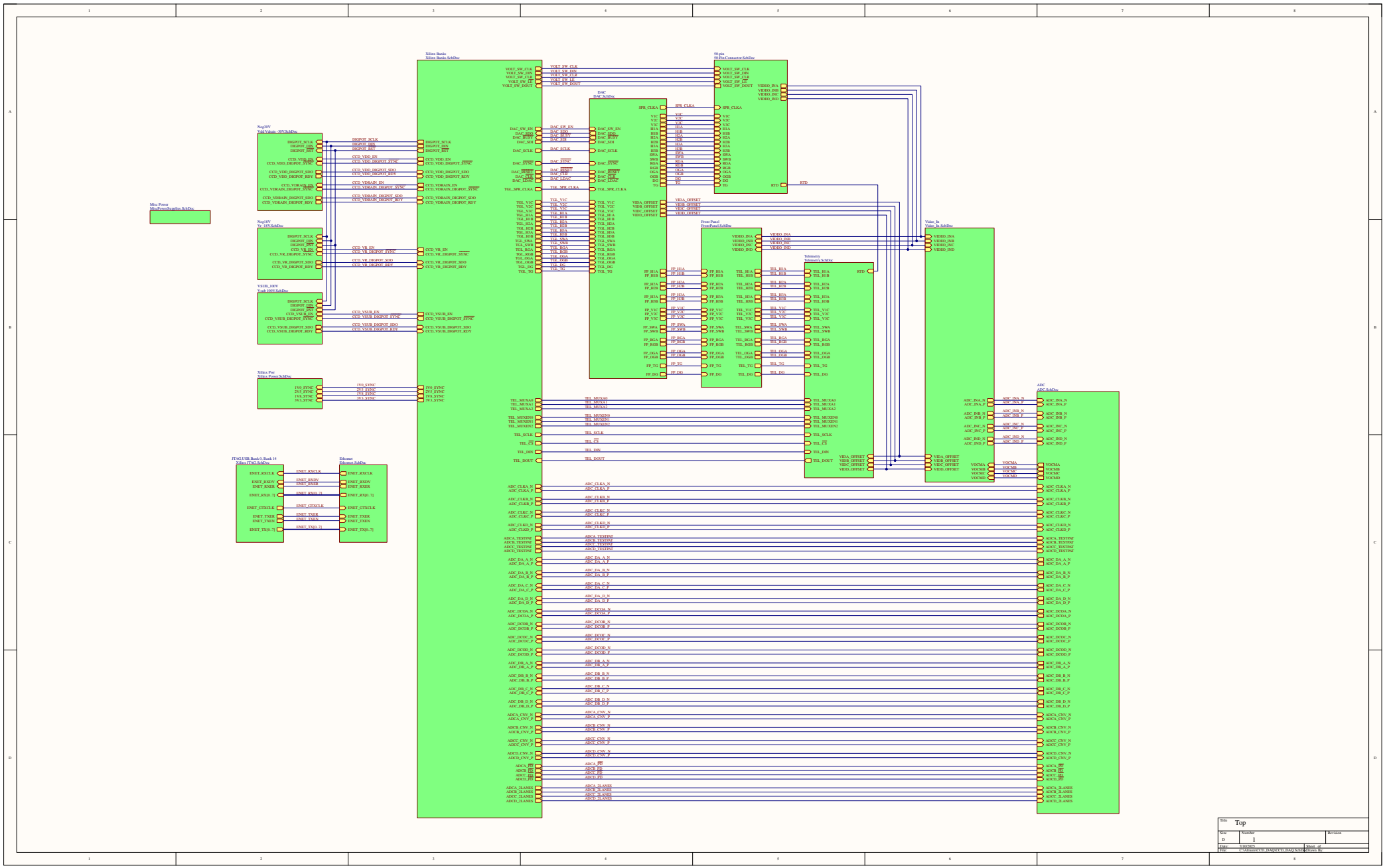
Xilinx Banks
Xilinx Banks.SchDoc
50-pin
50 Pin Connector.SchDoc
DAC
DAC.SchDoc
Front Panel
FrontPanel.SchDoc
Telemetry
Telemetry.SchDoc
Video_In
Video_In.SchDoc
ADC
ADC.SchDoc
Misc Power
MiscPowerSupplies.SchDoc
Xilinx Pwr
Xilinx Power.SchDoc
JTAG/USB Bank 0, Bank 14
Xilinx JTAG.SchDoc
Ethernet
Ethernet.SchDoc
Top
Size
D
Number
1
Revision
Date:
7/10/2025
Sheet of
File:
C:\Altium\CCD_DAQ\CCD_DAQ.SchDoc
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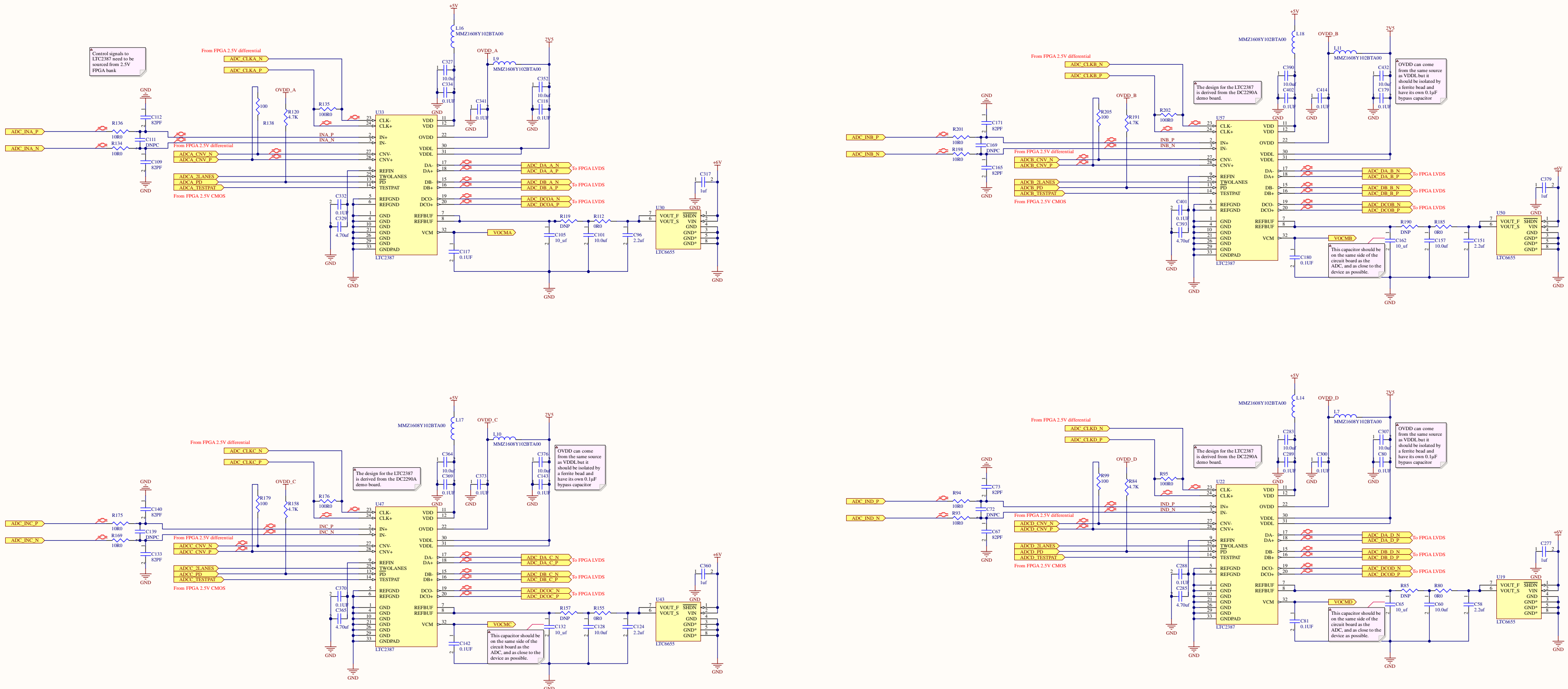

Title ADC

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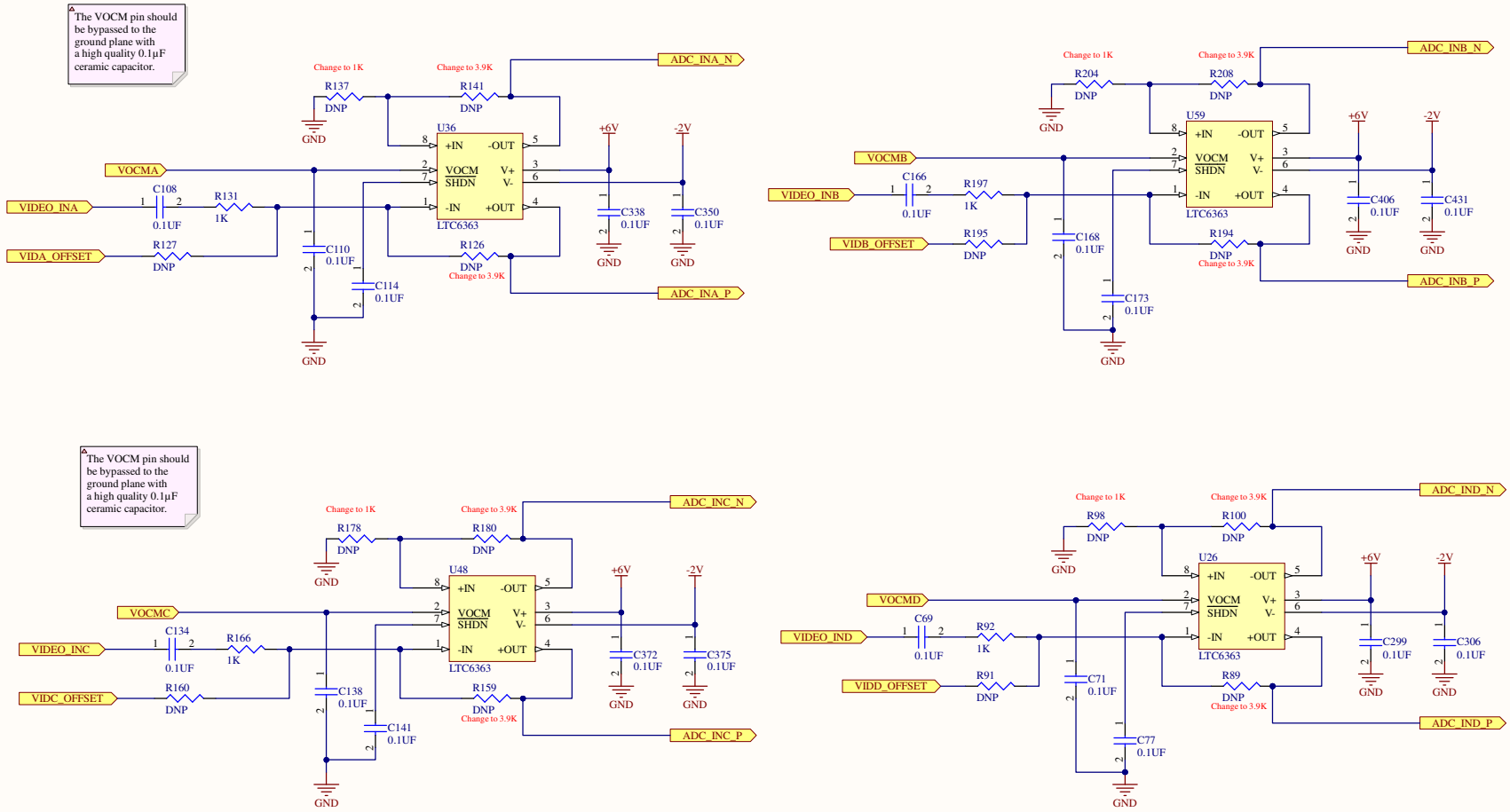
File: C:\Altium\CCD_DAQ\ADC.SchDoc | Drawn By:


The VOCM pin should be bypassed to the ground plane with a high quality 0.1µF ceramic capacitor.
Change to 1K
Change to 3.9K
R137
DNP
R141
DNP
ADC_INA_N
U36
+IN
-OUT
VOCM
V+
SHDN
V-
-IN
+OUT
LTC6363
+6V
-2V
VOCMA
VIDEO_INA
C108
0.1UF
R131
1K
VIDA_OFFSET
R127
DNP
C110
0.1UF
C114
0.1UF
R126
DNP
Change to 3.9K
C338
0.1UF
C350
0.1UF
ADC_INA_P
GND
Change to 1K
Change to 3.9K
R204
DNP
R208
DNP
ADC_INB_N
U59
VOCMB
VIDEO_INB
C166
0.1UF
R197
1K
VIDB_OFFSET
R195
DNP
C168
0.1UF
C173
0.1UF
R194
DNP
Change to 3.9K
C406
0.1UF
C431
0.1UF
ADC_INB_P
The VOCM pin should be bypassed to the ground plane with a high quality 0.1µF ceramic capacitor.
Change to 1K
Change to 3.9K
R178
DNP
R180
DNP
ADC_INC_N
U48
VOCMC
VIDEO_INC
C134
0.1UF
R166
1K
VIDC_OFFSET
R160
DNP
C138
0.1UF
C141
0.1UF
R159
DNP
Change to 3.9K
C372
0.1UF
C375
0.1UF
ADC_INC_P
Change to 1K
Change to 3.9K
R98
DNP
R100
DNP
ADC_IND_N
U26
VOCMD
VIDEO_IND
C69
0.1UF
R92
1K
VIDD_OFFSET
R91
DNP
C71
0.1UF
C77
0.1UF
R89
DNP
Change to 3.9K
C299
0.1UF
C306
0.1UF
ADC_IND_P
Title
Video In
Size
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Number
3
Revision
Date:
7/10/2025
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File:
C:\Altium\CCD_DAQ\Video_In.SchDoc
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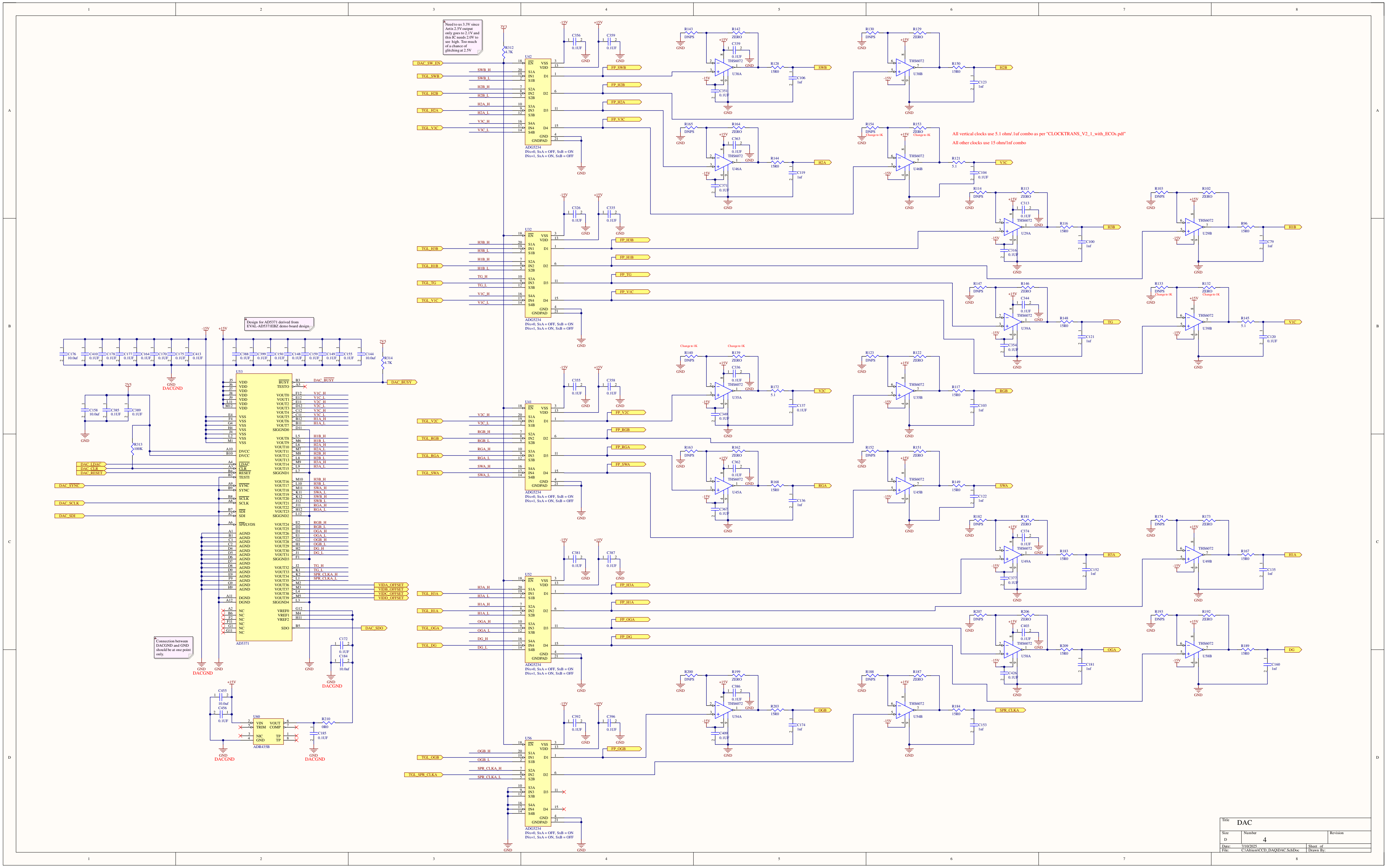
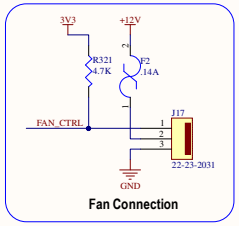
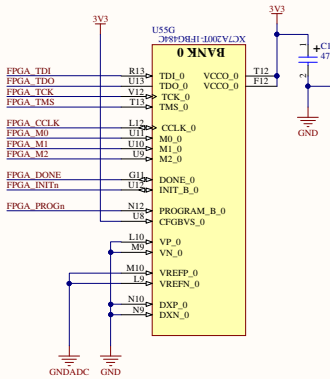
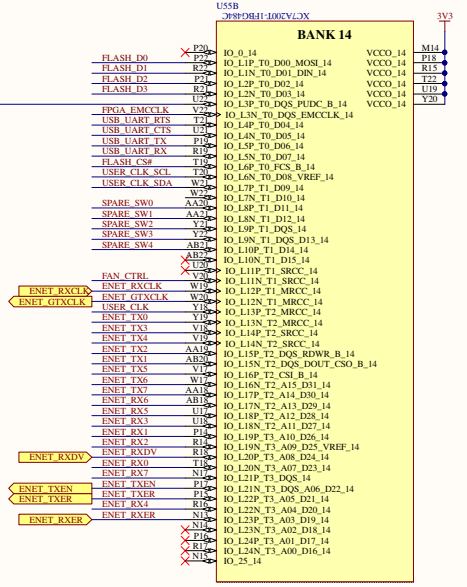
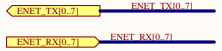
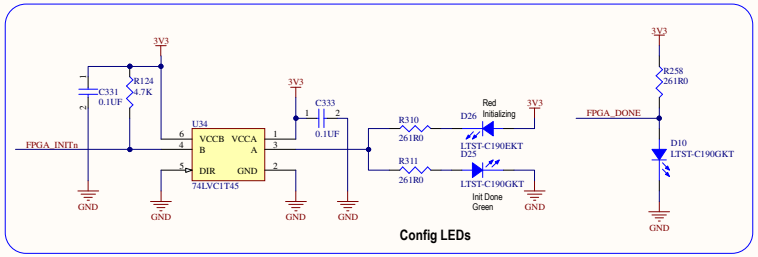

Need to us 3.3V since Artix 2.5V output only goes to 2.1V and this IC needs 2.0V to see high. Too much of a chance of glitching at 2.5V
Design for AD5371 derived from EVAL-AD5371EBZ demo board design
Connection between DACGND and GND should be at one point only.
All vertical clocks use 5.1 ohm/.1uf combo as per "CLOCKTRANS_V2_1_with_ECOs.pdf"
All other clocks use 15 ohm/1nf combo
ADG5234
INx=0, SxA = OFF, SxB = ON
INx=1, SxA = ON, SxB = OFF
AD5371
ADR435B
THS6072
DAC_SW_EN
DAC_BUSY
DAC_LDAC
DAC_CLR
DAC_RESET
DAC_SYNC
DAC_SCLK
DAC_SDI
DAC_SDO
VIDA_OFFSET
VIDB_OFFSET
VIDC_OFFSET
VIDD_OFFSET
DACGND
Title DAC
Size D
Number 4
Date: 7/10/2025
File: C:\Altium\CCD_DAQ\DAC.SchDoc
Revision
Sheet of
Drawn By:

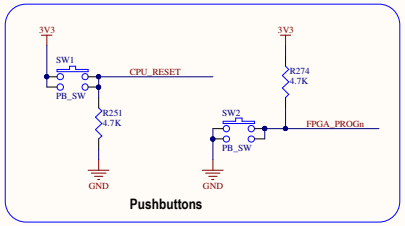


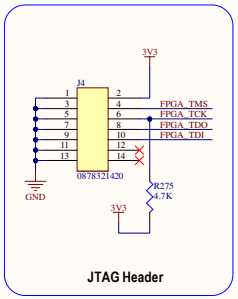


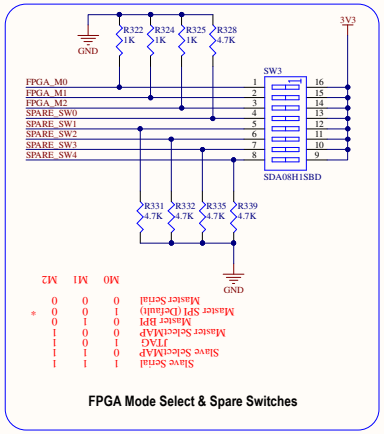


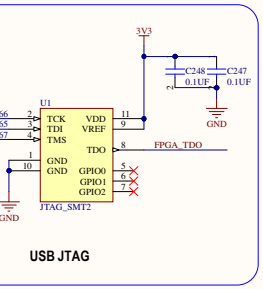


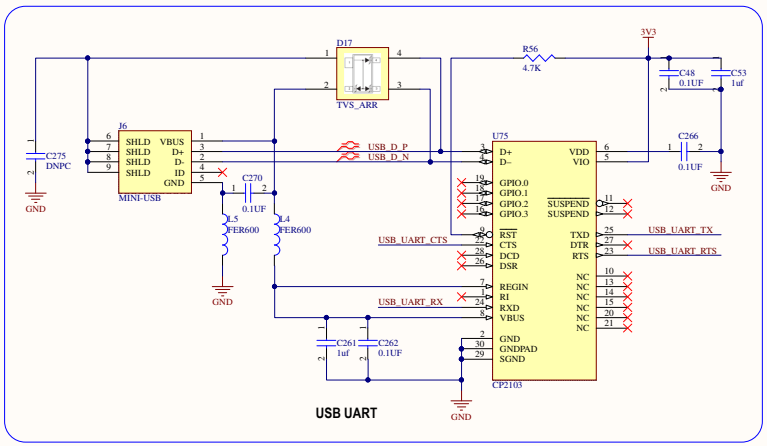


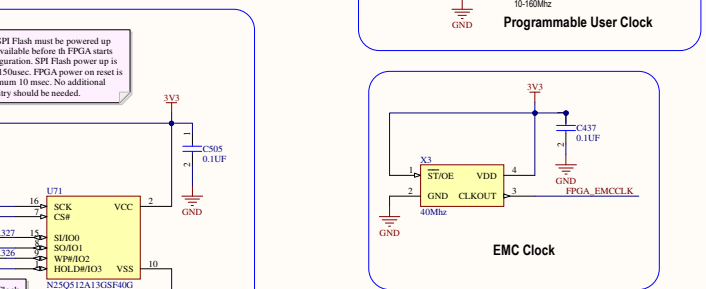


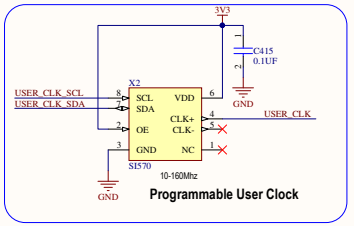










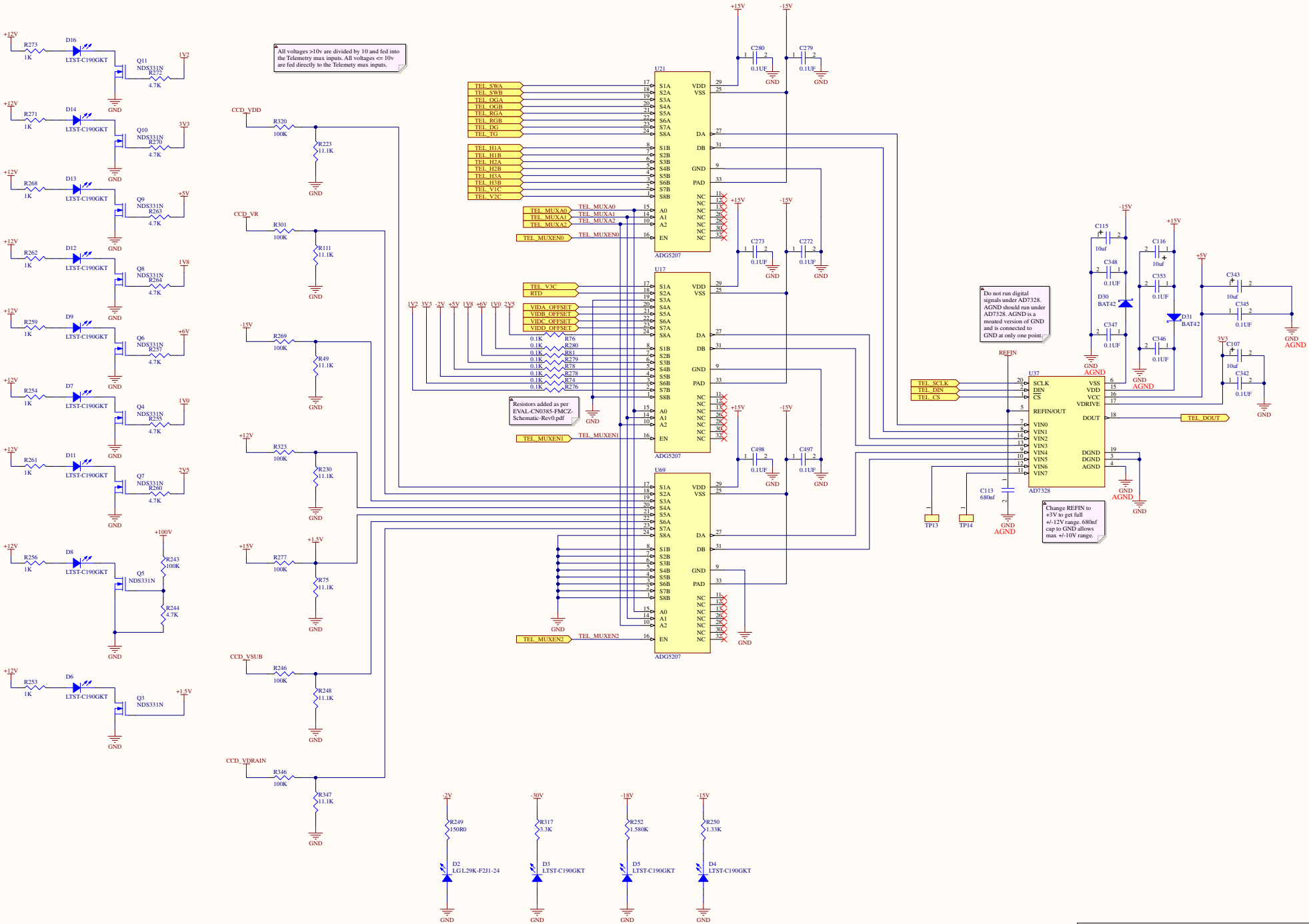


Title: JTAG, USB , Flash, Bank 0, Ethernet, Bank 14

Size	Number	Revision
C	5	

Date: 7/10/2025 Sheet of

File: C:\Altium\CCD_DAQ\Xilinx JTAG.SchDoc Drawn By:


All voltages >10v are divided by 10 and fed into the Telemetry mux inputs. All voltages <= 10v are fed directly to the Telemetry mux inputs.
Resistors added as per EVAL-CN0385-FMCZ-Schematic-Rev0.pdf
Do not run digital signals under AD7328. AGND should run under AD7328. AGND is a moated version of GND and is connected to GND at only one point.
Change REFIN to +3V to get full +/-12V range. 680nf cap to GND allows max +/-10V range.
U21
U17
U69
ADG5207
U37
AD7328
TEL_SWA
TEL_SWB
TEL_OGA
TEL_OGB
TEL_RGA
TEL_RGB
TEL_DG
TEL_TG
TEL_H1A
TEL_H1B
TEL_H2A
TEL_H2B
TEL_H3A
TEL_H3B
TEL_V1C
TEL_V2C
TEL_V3C
RTD
TEL_MUXA0
TEL_MUXA1
TEL_MUXA2
TEL_MUXEN0
TEL_MUXEN1
TEL_MUXEN2
VIDA_OFFSET
VIDB_OFFSET
VIDC_OFFSET
VIDD_OFFSET
TEL_SCLK
TEL_DIN
TEL_CS
TEL_DOUT
REFIN
CCD_VDD
CCD_VR
CCD_VSUB
CCD_VDRAIN
Title
Telemetry
Size
C
Number
6
Revision
Date:
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File:
C:\Altium\CCD_DAQ\Telemetry.SchDoc
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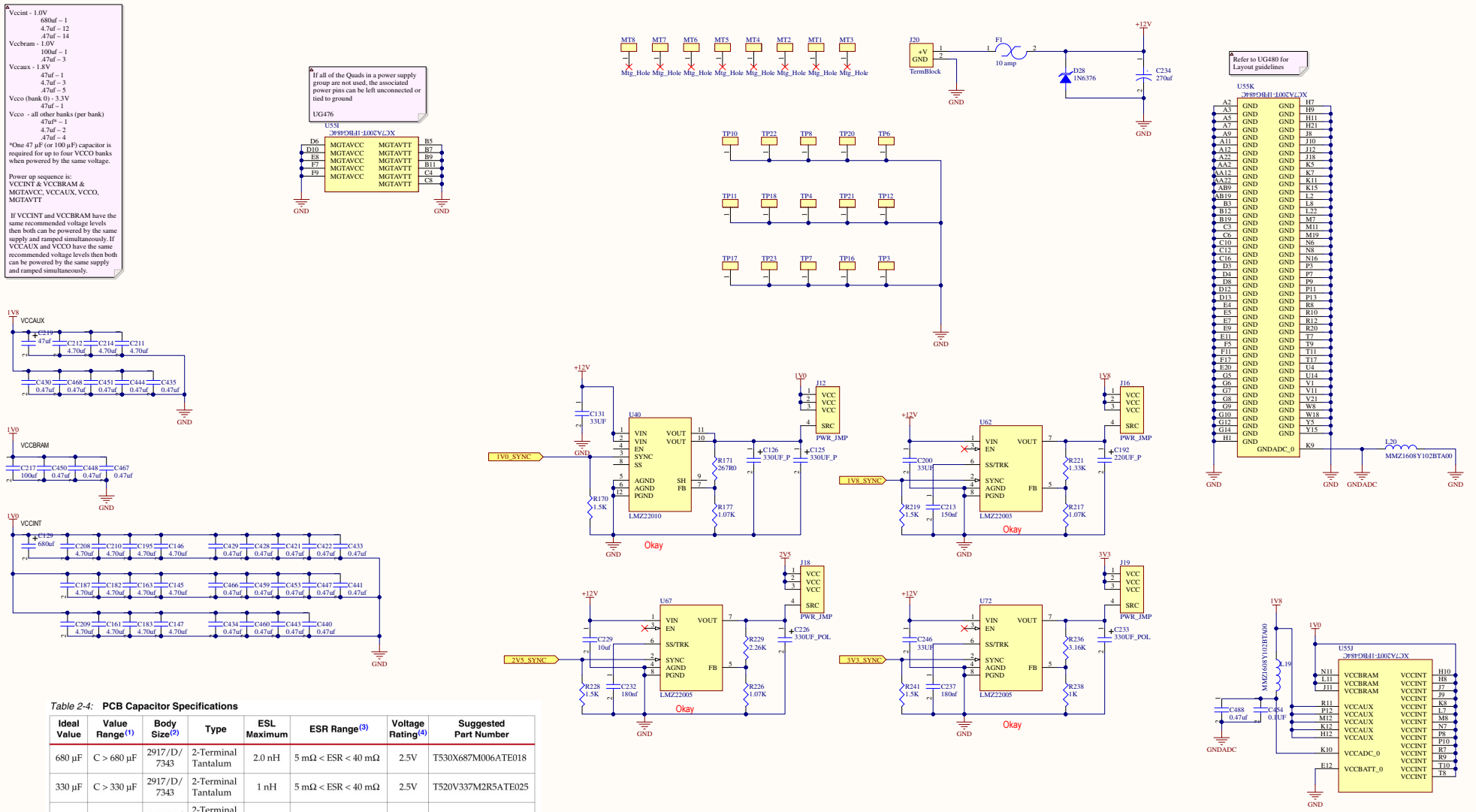


Table 2-4: **PCB Capacitor Specifications**

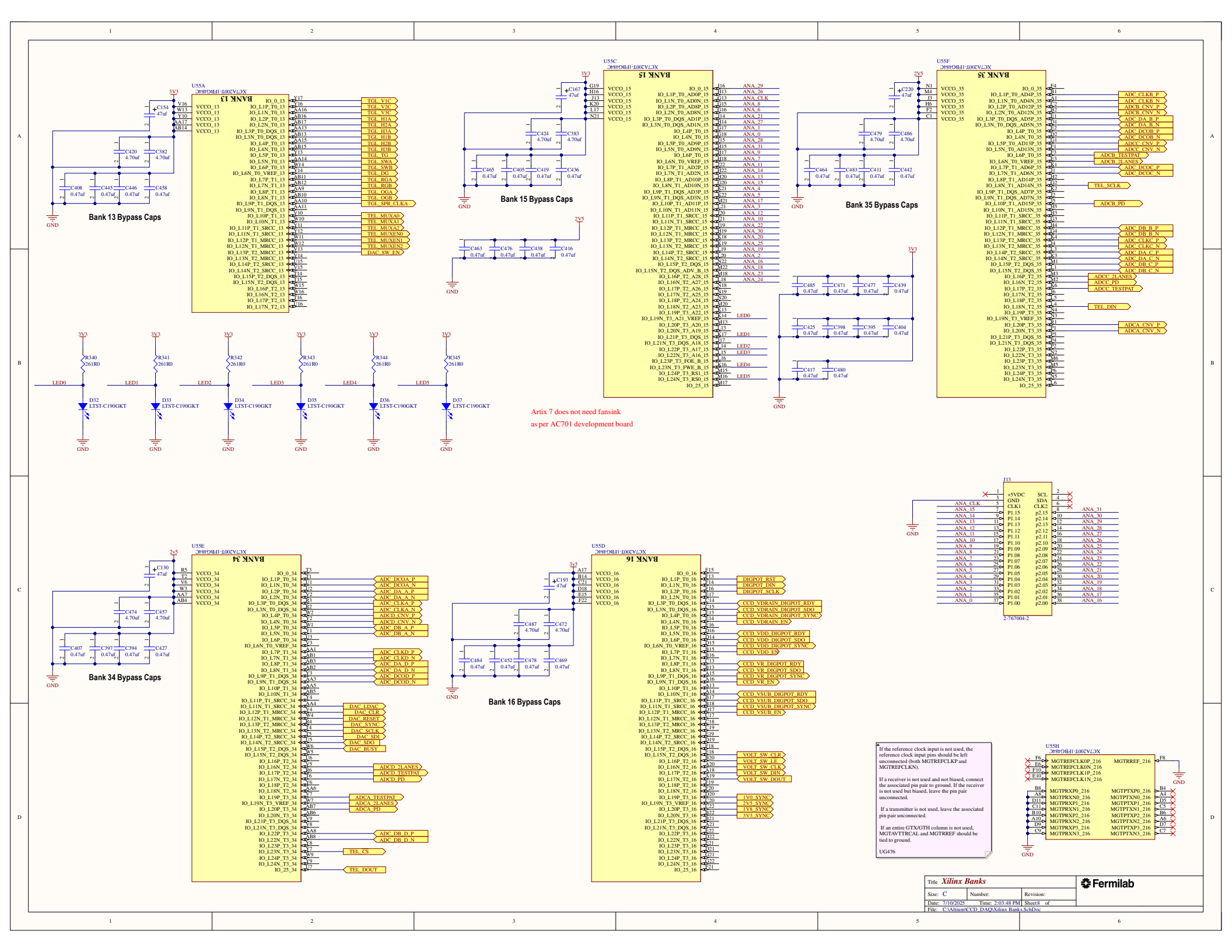
Ideal Value	Value Range[1]	Body Size[2]	Type	ESL Maximum	ESR Range[3]	Voltage Rating[4]	Suggested Part Number
680 µF	C > 680 µF	2917/D/7343	2-Terminal Tantalum	2.0 nH	5 mΩ < ESR < 40 mΩ	2.5V	T530X687M006ATE018
330 µF	C > 330 µF	2917/D/7343	2-Terminal Tantalum	1 nH	5 mΩ < ESR < 40 mΩ	2.5V	T520V337M2R5ATE025
330 µF	C > 330 µF	2917/D/7343	2-Terminal Niobium Oxide	1 nH	5 mΩ < ESR < 100 mΩ	2.5V	NOSD337M002#0035
100 µF	C > 100 µF	1210	2-Terminal Tantalum Ceramic X7R or X5R	1 nH	1 mΩ < ESR < 40 mΩ	2.5V	GRM32ER60J107ME20L
47 µF	C > 47 µF	1210	2-Terminal Ceramic X7R or X5R	1 nH	1 mΩ < ESR < 40 mΩ	6.3V	GRM32ER70J476ME20L
4.7 µF	C > 4.7 µF	0805	2-Terminal Ceramic X7R or X5R	0.5 nH	1 mΩ < ESR < 20 mΩ	6.3V	GRM21BR71A475KA73

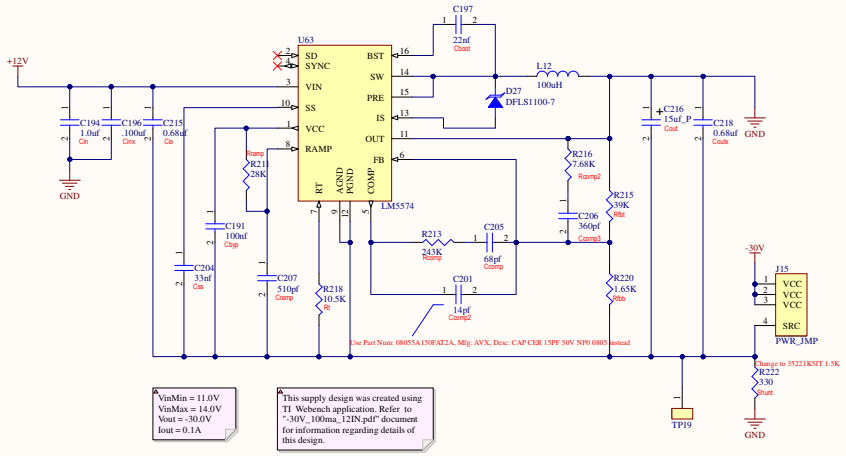
Ideal Value	Value Range[1]	Body Size[2]	Type	ESL Maximum	ESR Range[3]	Voltage Rating[4]	Suggested Part Number
0.47 µF	C > 0.47 µF	0603	2-Terminal Ceramic X7R or X5R	0.5 nH	1 mΩ < ESR < 20 mΩ	6.3V	GRM188R70J474KA01

Table 2-1: **Required PCB Capacitor Quantities per Device: Artix-7 Devices[1][2]**

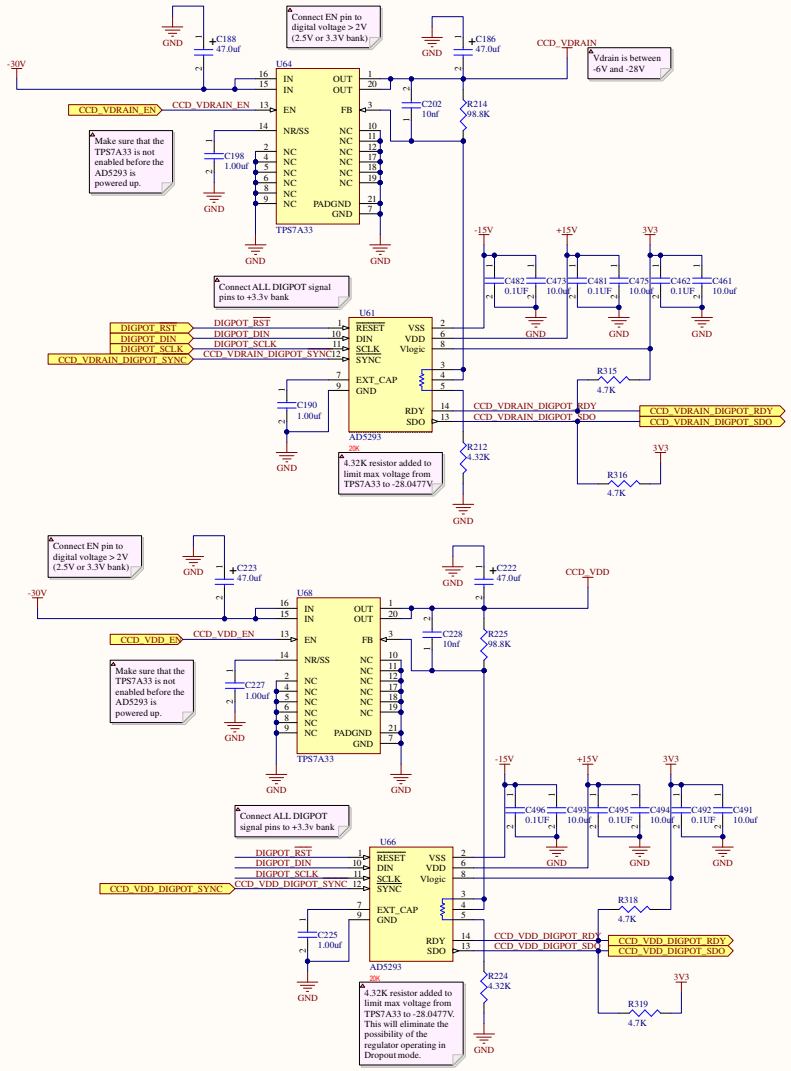
Package	Device	V_{CCINT}						V_{CCBRAM}				V_{CCAUX}			V_{CCO} Bank 0	V_{CCO} all other Banks (per Bank)		
		680 µF	330 µF	100 µF	47 µF	4.7 µF	0.47 µF	100 µF	47 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	0.47 µF	47 µF	47 µF or 100 µF[3]	4.7 µF	0.47 µF
FBG484 FBV484 RB484	XC7A200T XQ7A200T	1	0	0	0	12	14	1	0	0	3	1	3	5	1	1	2	4

Title	Xilinx Power		
Size C	Number 7		Revision
Date: 7/10/2025		Sheet of	
File: C:\Altium\CCD_DAQ\Xilinx Power.SchDoc		Drawn By:	

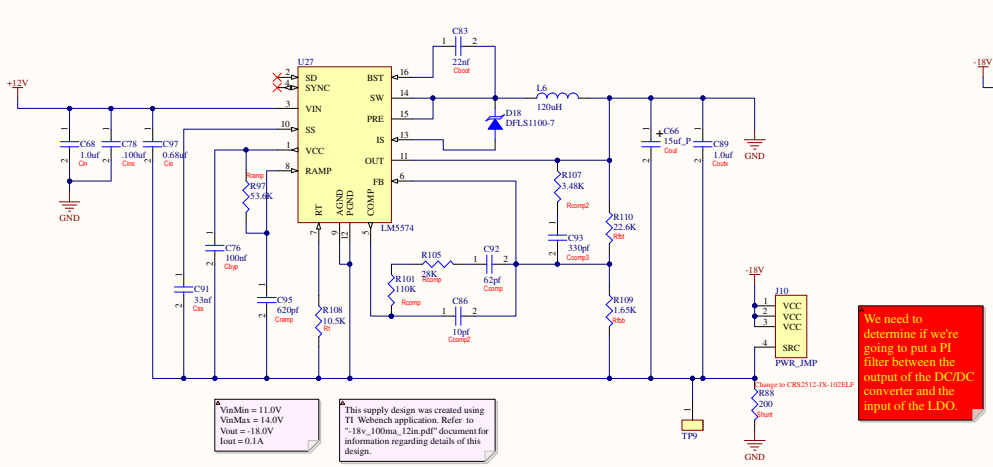

Bank 13 Bypass Caps
Bank 15 Bypass Caps
Bank 35 Bypass Caps
Bank 34 Bypass Caps
Bank 16 Bypass Caps
Artix 7 does not need fansink
as per AC701 development board
If the reference clock input is not used, the reference clock input pins should be left unconnected (both MGTREFCLKP and MGTREFCLKN).
If a receiver is not used and not biased, connect the associated pin pair to ground. If the receiver is not used but biased, leave the pin pair unconnected.
If a transmitter is not used, leave the associated pin pair unconnected.
If an entire GTX/GTH column is not used, MGTAVTTRCAL and MGTRREF should be tied to ground.
UG476
Title Xilinx Banks
Size: C
Number:
Revision:
Date: 7/10/2025
Time: 2:03:48 PM
Sheet8 of
File: C:\Altium\CCD_DAQ\Xilinx Banks.SchDoc
Fermilab

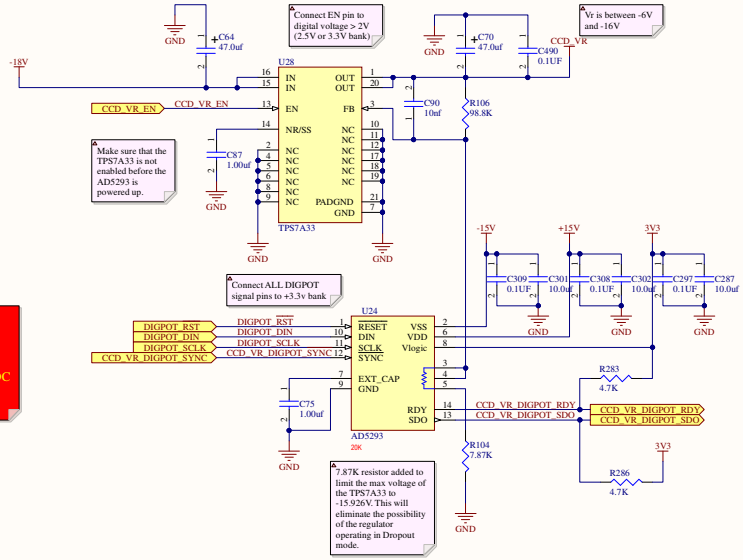


We need to determine if we're going to put a PI filter between the output of the DC/DC converter and the input of the LDO.

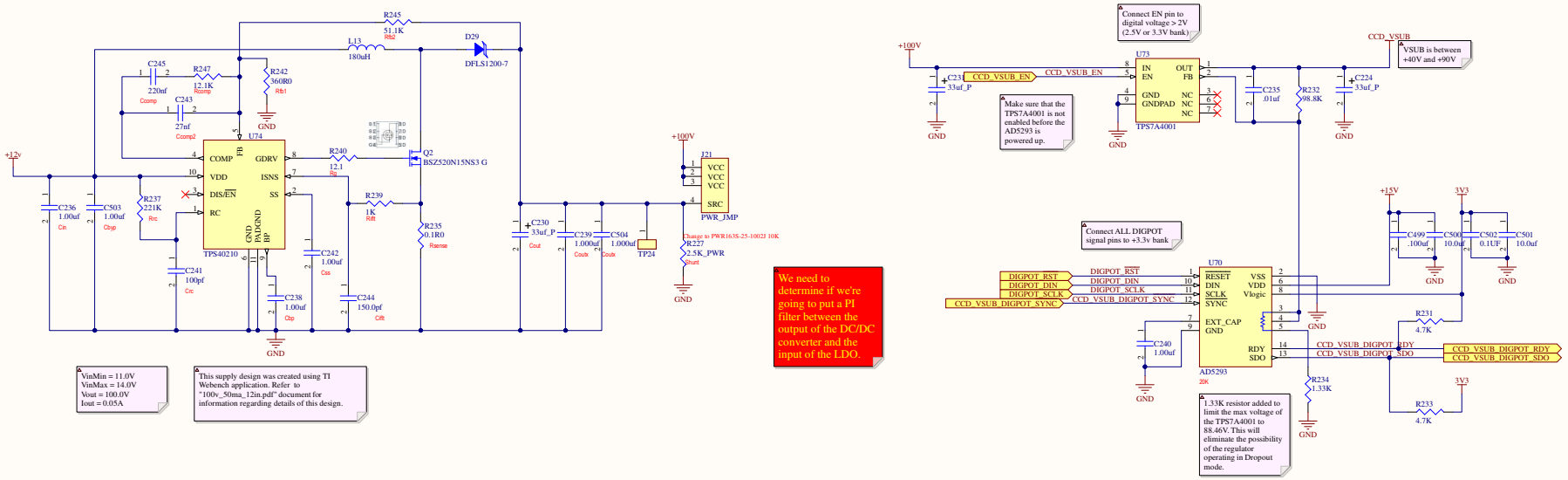


Title: *Vdd Vdrain -30V*		Fermilab
Size: C	Number:	Revision:
Date: 7/10/2025	Time: 2:03:49 PM	Sheet9 of
File: C:\Altium\CCD_DAQ\Vdd Vdrain -30V.SchDoc		

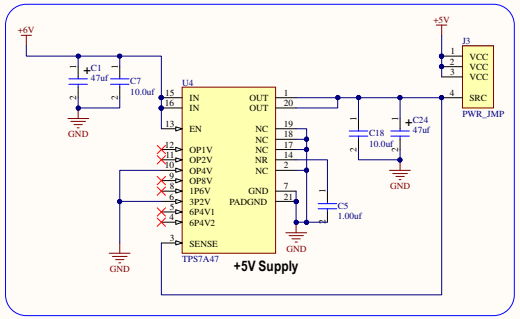


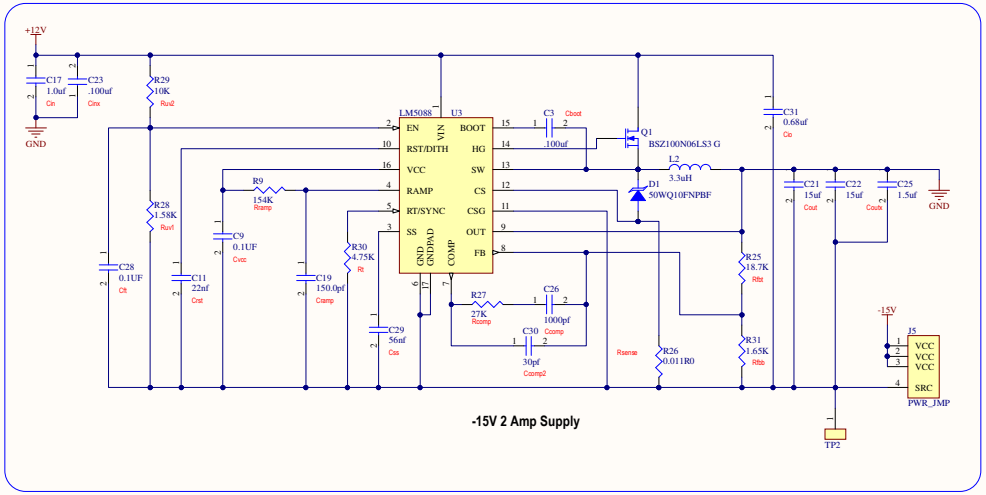


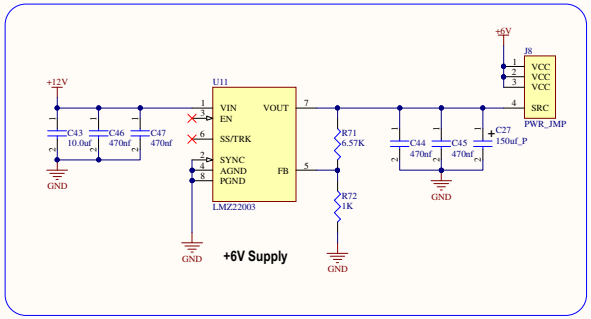
Title	*Vr -18V*		Fermilab
Size: C	Number:	Revision:	
Date: 7/10/2025	Time: 2:03:50 PM	Sheet 10 of	
File: C:\Altium\CCD_DAQ\Vr -18V.SchDoc			

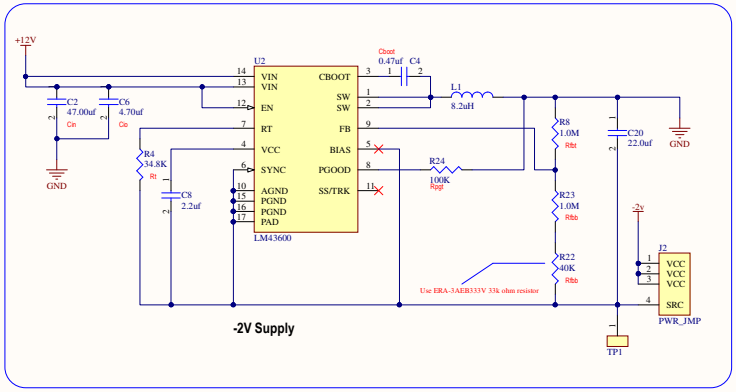


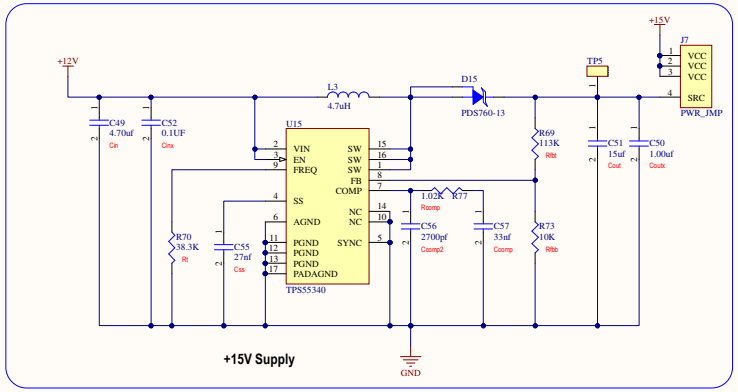
Title	*VSUB +100v*		Fermilab
Size: C	Number:	Revision:	
Date: 7/10/2025	Time: 2:03:51 PM	Sheet 11 of	
File: C:\Altium\CCD_DAQ\Vsub 100V.SchDoc			



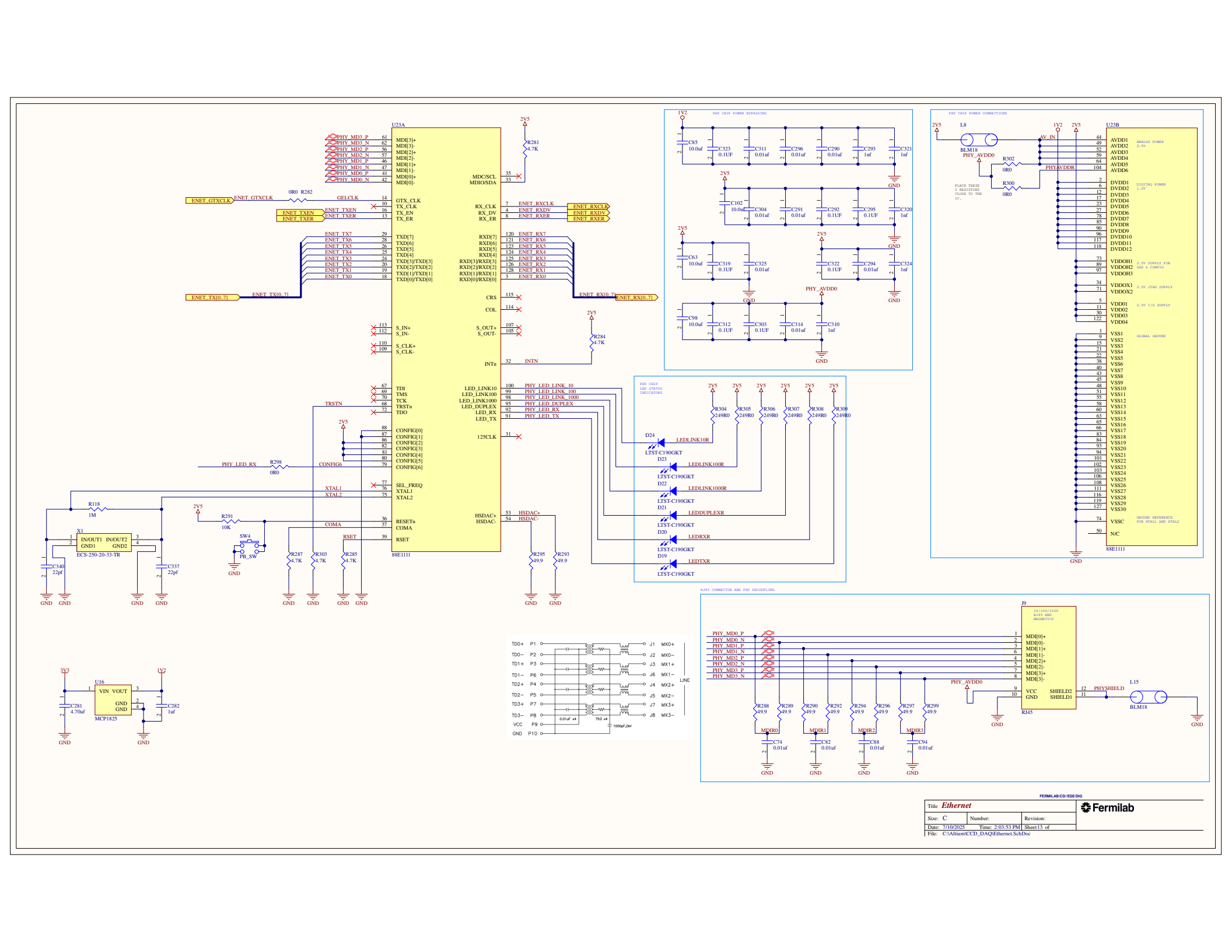


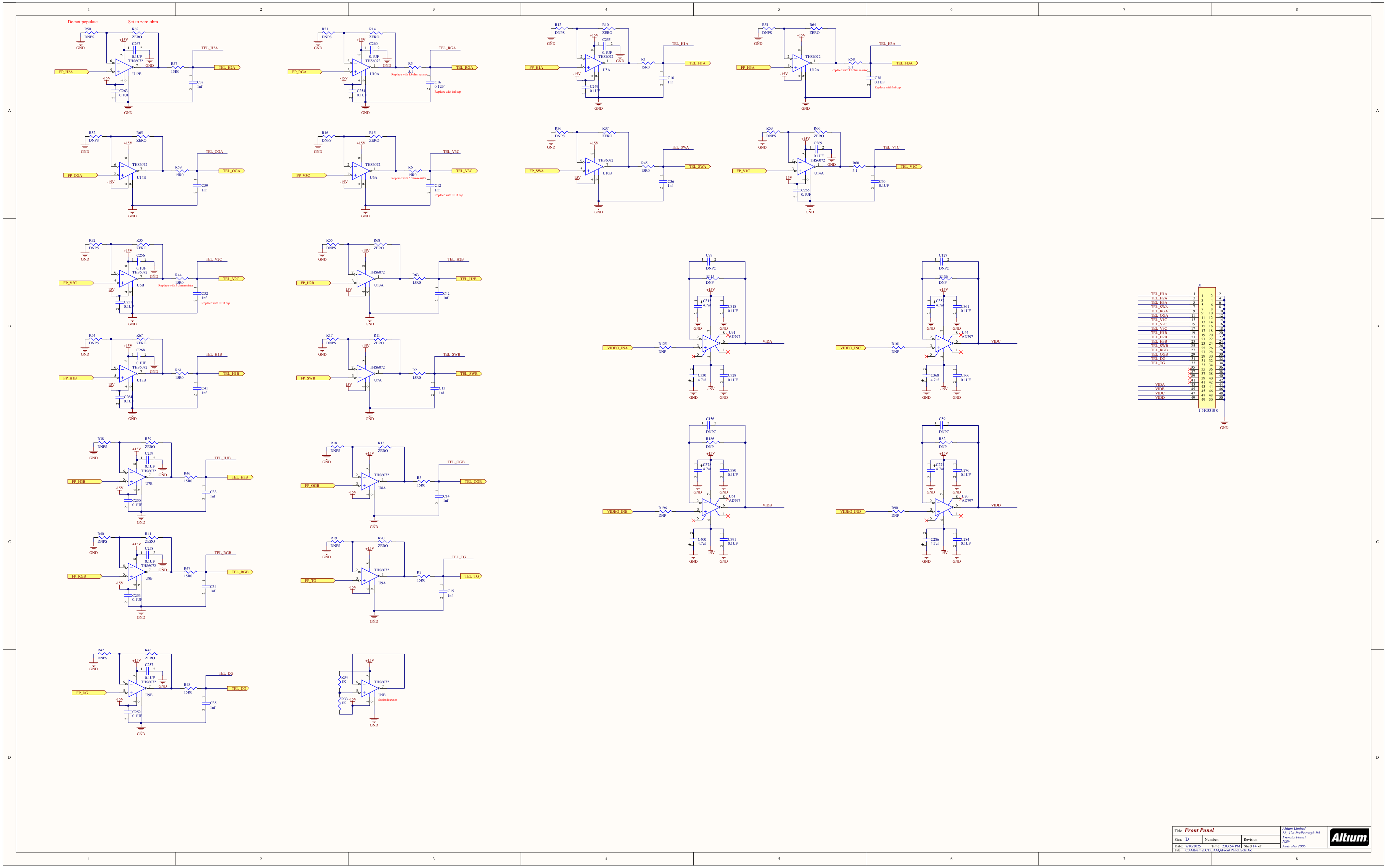






Title: *Misc Power Supplies*		Fermilab
Size: C	Number:	Revision:
Date: 7/10/2025	Time: 2:03:52 PM	Sheet 12 of
File: C:\Altium\CCD_DAQ\MiscPowerSupplies.SchDoc		


U23A
88E1111
PHY_MD3_P
PHY_MD3_N
PHY_MD2_P
PHY_MD2_N
PHY_MD1_P
PHY_MD1_N
PHY_MD0_P
PHY_MD0_N
MDI[3]+
MDI[3]-
MDI[2]+
MDI[2]-
MDI[1]+
MDI[1]-
MDI[0]+
MDI[0]-
MDC/SCL
MDIO/SDA
R281
4.7K
2V5
0R0 R282
ENET_GTXCLK
GELCLK
GTX_CLK
TX_CLK
TX_EN
TX_ER
RX_CLK
RX_DV
RX_ER
ENET_TXEN
ENET_TXER
ENET_RXCLK
ENET_RXDV
ENET_RXER
ENET_TX7
ENET_TX6
ENET_TX5
ENET_TX4
ENET_TX3
ENET_TX2
ENET_TX1
ENET_TX0
TXD[7]
TXD[6]
TXD[5]
TXD[4]
TXD[3]/TXD[3]
TXD[2]/TXD[2]
TXD[1]/TXD[1]
TXD[0]/TXD[0]
RXD[7]
RXD[6]
RXD[5]
RXD[4]
RXD[3]/RXD[3]
RXD[2]/RXD[2]
RXD[1]/RXD[1]
RXD[0]/RXD[0]
ENET_RX7
ENET_RX6
ENET_RX5
ENET_RX4
ENET_RX3
ENET_RX2
ENET_RX1
ENET_RX0
ENET_TX[0..7]
ENET_RX[0..7]
CRS
COL
S_IN+
S_IN-
S_CLK+
S_CLK-
S_OUT+
S_OUT-
R284
4.7K
INTn
INTN
TDI
TMS
TCK
TRSTn
TDO
TRSTN
LED_LINK10
LED_LINK100
LED_LINK1000
LED_DUPLEX
LED_RX
LED_TX
PHY_LED_LINK_10
PHY_LED_LINK_100
PHY_LED_LINK_1000
PHY_LED_DUPLEX
PHY_LED_RX
PHY_LED_TX
125CLK
CONFIG[0]
CONFIG[1]
CONFIG[2]
CONFIG[3]
CONFIG[4]
CONFIG[5]
CONFIG[6]
PHY_LED_RX
R298
0R0
CONFIG6
SEL_FREQ
XTAL1
XTAL2
R118
1M
X1
ECS-250-20-33-TR
C340
22pf
C337
22pf
R291
10K
COMA
RESETn
RSET
SW4
PB_SW
R287
4.7K
R303
4.7K
R285
4.7K
HSDAC+
HSDAC-
R295
49.9
R293
49.9
GND
PHY CHIP POWER BYPASSING
C85
10.0uf
C323
0.1UF
C311
0.01uf
C296
0.01uf
C290
0.01uf
C293
1nf
C321
1nf
C102
10.0uf
C304
0.01uf
C291
0.01uf
C292
0.1UF
C295
0.1UF
C320
1nf
C63
10.0uf
C319
0.1UF
C325
0.01uf
C322
0.1UF
C294
0.01uf
C324
1nf
C98
10.0uf
C312
0.1UF
C303
0.1UF
C314
0.01uf
C310
1nf
PHY_AVDD0
PHY CHIP POWER CONNECTIONS
L8
BLM18
PHY_AVDD0
R302
0R0
R300
0R0
PLACE THESE 2 RESISTORS CLOSE TO THE IC.
U23B
AV_IN
PHYAVDDR
AVDD1
AVDD2
AVDD3
AVDD4
AVDD5
AVDD6
ANALOG POWER 2.5V
DVDD1
DVDD2
DVDD3
DVDD4
DVDD5
DVDD6
DVDD7
DVDD8
DVDD9
DVDD10
DVDD11
DVDD12
DIGITAL POWER 1.2V
VDDOH1
VDDOH2
VDDOH3
2.5V SUPPLY FOR LED & CONFIG
VDDOX1
VDDOX2
2.5V JTAG SUPPLY
VDD01
VDD02
VDD03
VDD04
2.5V I/O SUPPLY
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS15
VSS16
VSS17
VSS18
VSS19
VSS20
VSS21
VSS22
VSS23
VSS24
VSS25
VSS26
VSS27
VSS28
VSS29
VSS30
GLOBAL GROUND
VSSC
GROUND REFERENCE FOR XTAL1 AND XTAL2
N/C
PHY CHIP LED STATUS INDICATORS
R304
249R0
R305
249R0
R306
249R0
R307
249R0
R308
249R0
R309
249R0
D24
LTST-C190GKT
LEDLINK10R
D23
LEDLINK100R
D22
LEDLINK1000R
D21
LEDDUPLEXR
D20
LEDRXR
D19
LEDTXR
3V3
U16
VIN VOUT
GND
MCP1825
C281
4.70uf
C282
1uf
1V2
RJ45 CONNECTOR AND PHY DECOUPLING
J9
10/100/1000 RJ45 AND MAGNETICS
MDI[0]+
MDI[0]-
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
MDI[3]+
MDI[3]-
VCC
SHIELD2
SHIELD1
RJ45
PHYSHIELD
L15
BLM18
R288
49.9
R289
49.9
R290
49.9
R292
49.9
R294
49.9
R296
49.9
R297
49.9
R299
49.9
MDIR0
MDIR1
MDIR2
MDIR3
C74
0.01uf
C82
0.01uf
C88
0.01uf
C94
0.01uf
TD0+ P1
TD0- P2
TD1+ P3
TD1- P6
TD2+ P4
TD2- P5
TD3+ P7
TD3- P8
VCC P9
GND P10
J1 MX0+
J2 MX0-
J3 MX1+
J6 MX1-
J4 MX2+
J5 MX2-
J7 MX3+
J8 MX3-
LINE
0.01uF x4
75Ω x4
1000pF,2kV
FERMILAB/CD/ESE/DIG
Title Ethernet
Size: C
Number:
Revision:
Date: 7/10/2025
Time: 2:03:53 PM
Sheet 13 of
File: C:\Altium\CCD_DAQ\Ethernet.SchDoc
Fermilab



Title: *Front Panel*

Size: D | Number: | Revision:

Date: 7/10/2025 Time: 2:03:54 PM Sheet 14 of

File: C:\Altium\CCD_DAQ\FrontPanel.SchDoc

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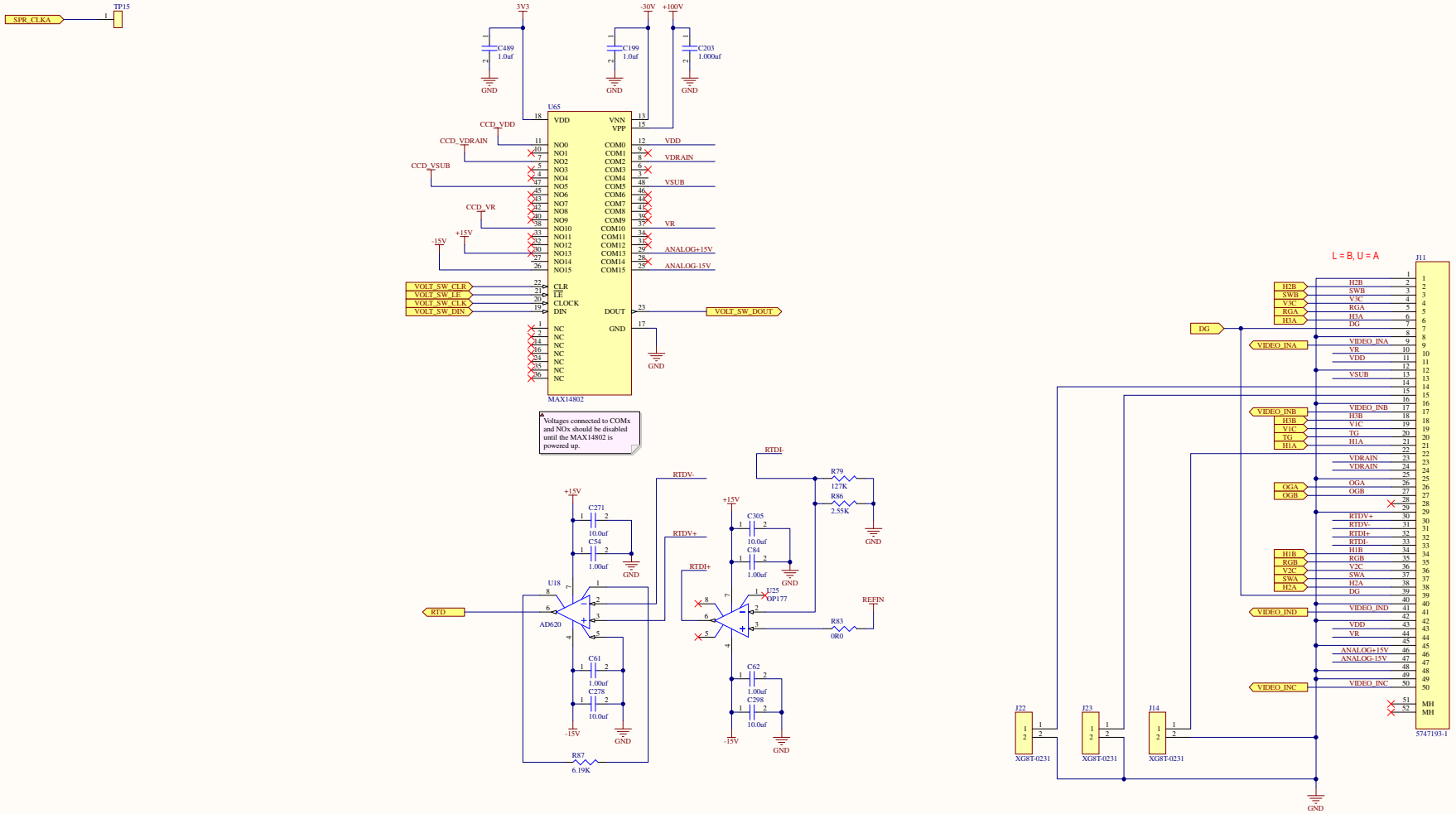
L3, 12a Rodborough Rd
Frenchs Forest
NSW
Australia 2086



Cannot open file C:\Altium\ccd_daq\RTD Circuit.png. File does not exist.

From document "12CH_Board_V3_Full_Schematics_with_ECOs-v4.pdf"

Title	50-Pin Connector		Altium Limited L3, 12a Rodborough Rd Frenchs Forest NSW Australia 2086
Size: Orcad C	Number:	Revision:	
Date: 7/10/2025	Time: 2:03:55 PM	Sheet 15 of	
File: C:\Altium\CCD_DAQ\50-Pin Connector.SchDoc			