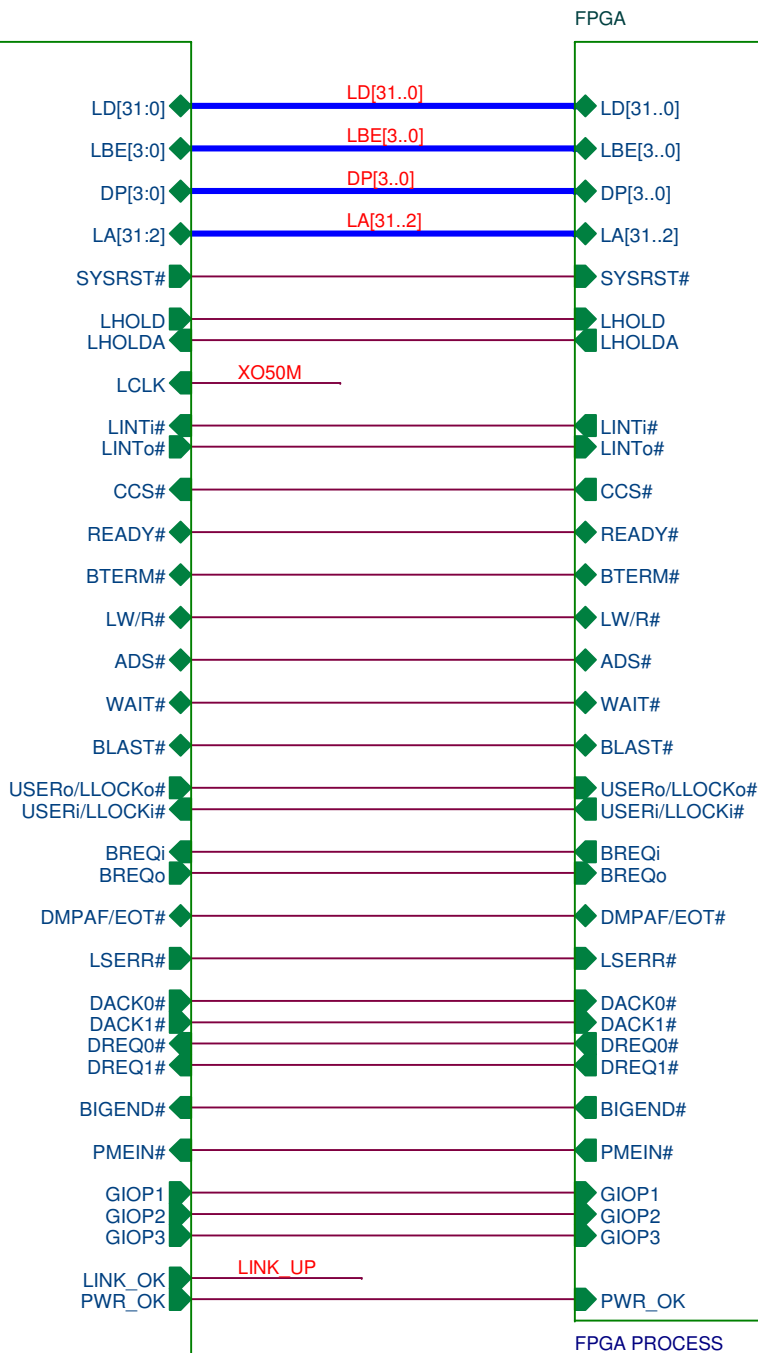
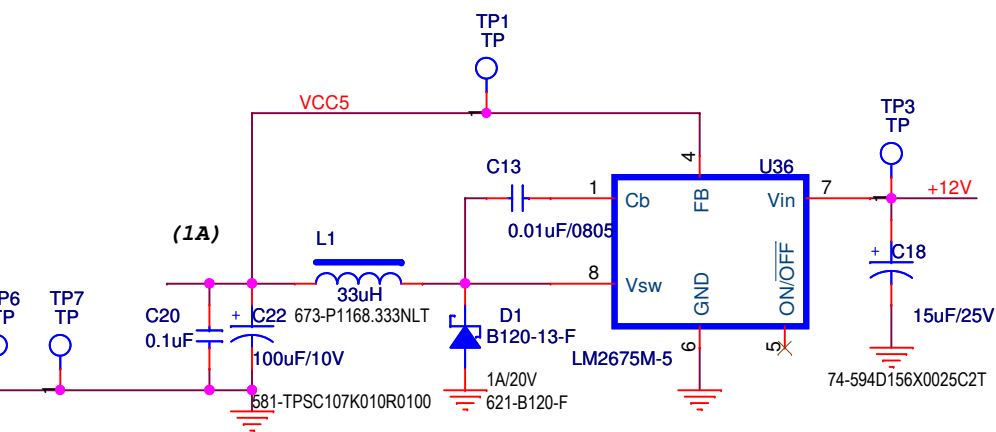
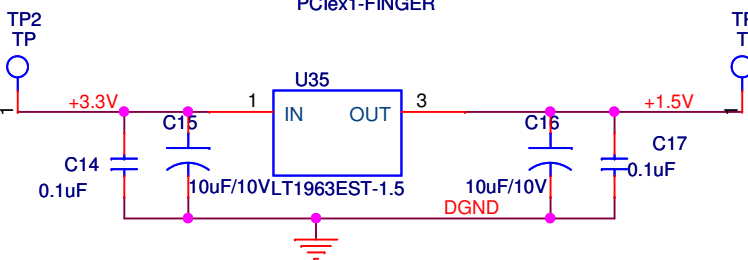
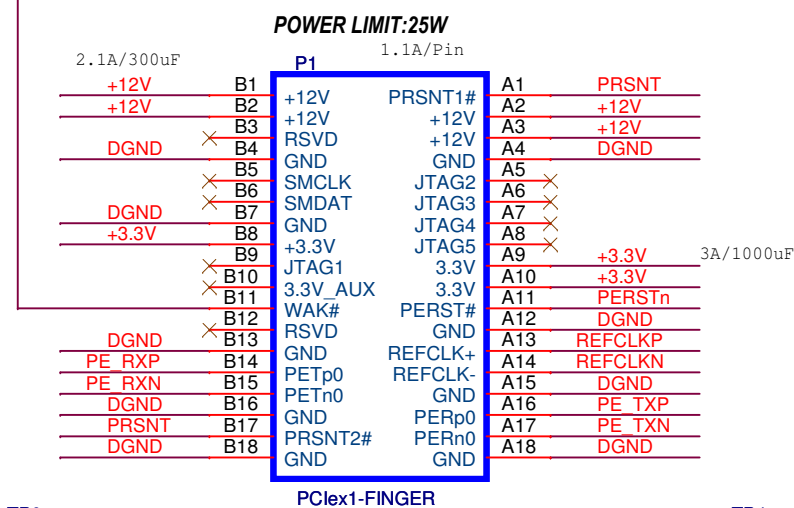
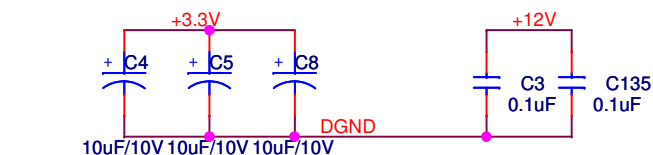
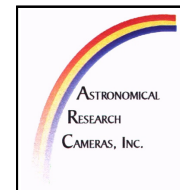
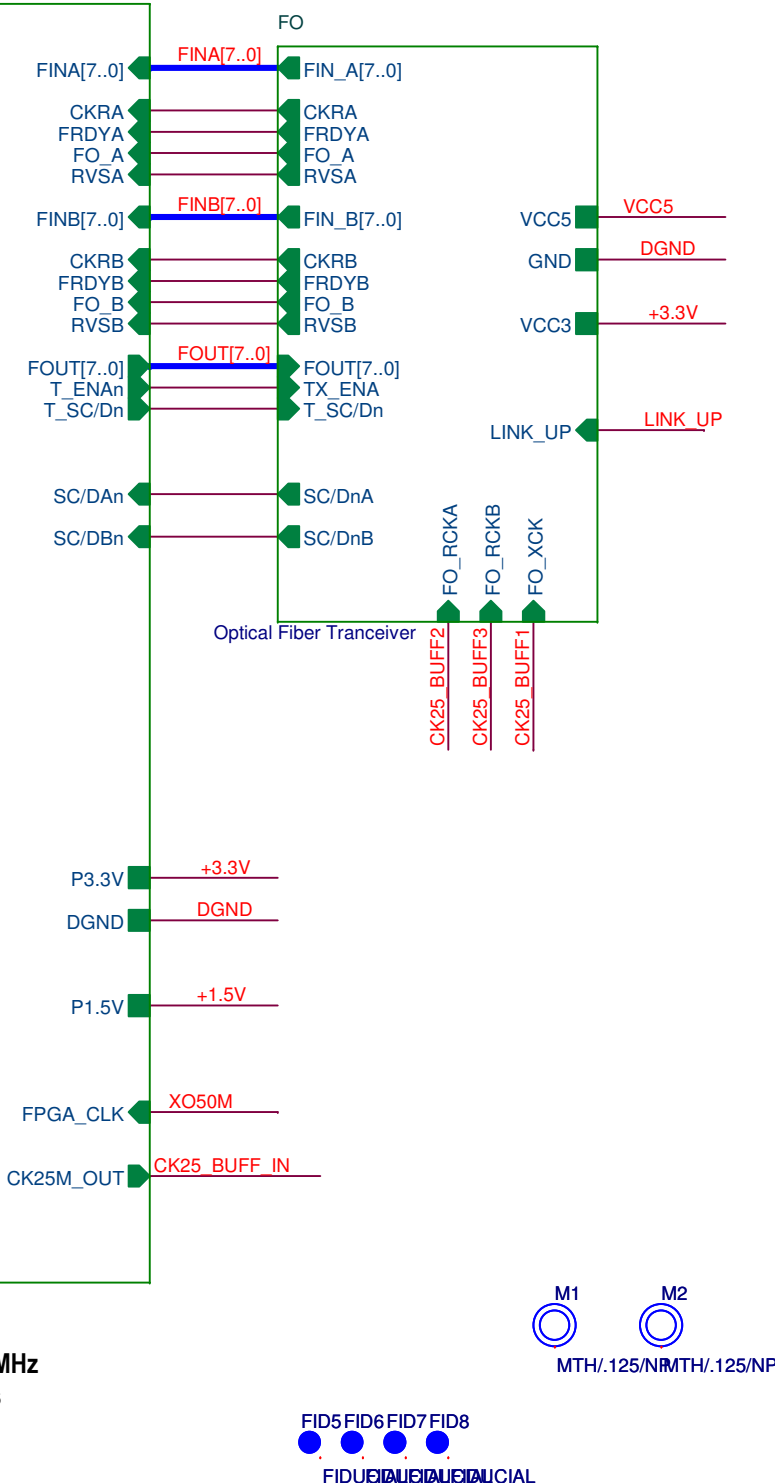
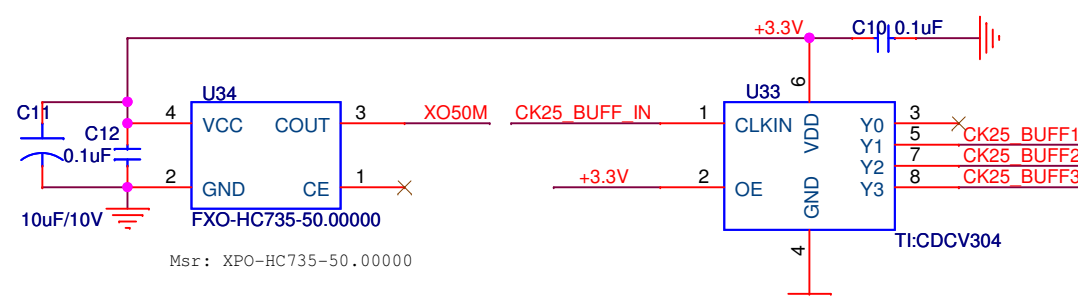


Differential pair trace length's difference be less than 5mil

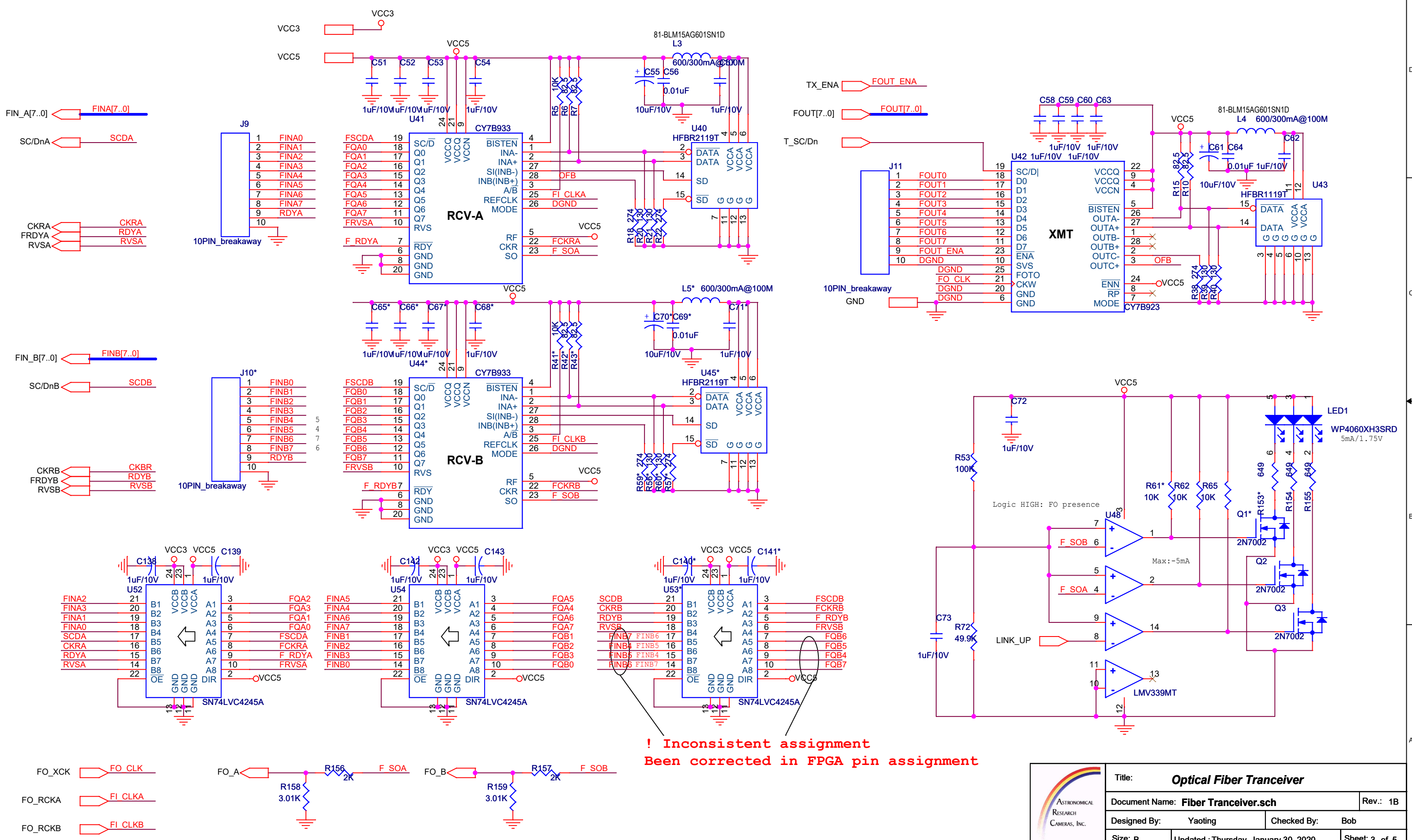
Place Cap within 250mil to the Transmitter



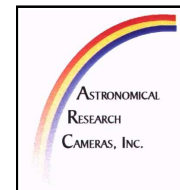
**EP1C6Q240C6**  
I/O Speed:>300MHz  
RAM: 52x4Kbits



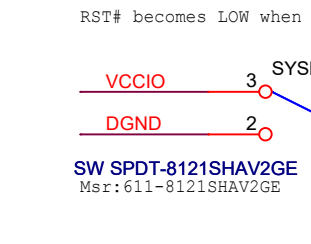
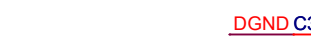
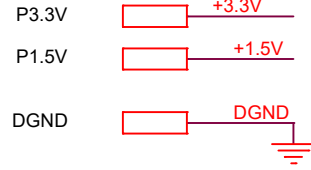
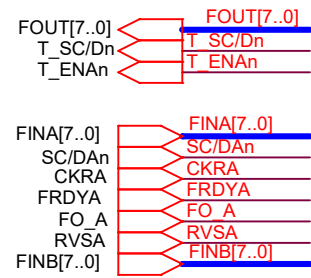
Title: <b>ARC-66 PCI Express Card</b>			
Document Name: <b>sch_1A.sch</b>		Rev.: 1B	
Designed By: <b>Yaoting</b>	Checked By: <b>Bob</b>		
Size: B	Updated: Friday, June 03, 2011	Sheet: 1 of 5	



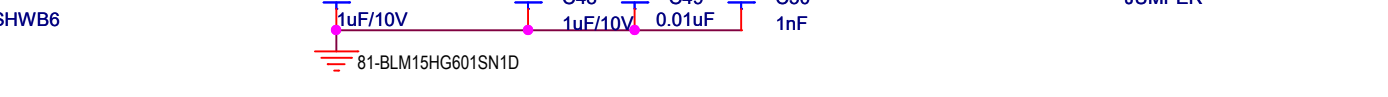
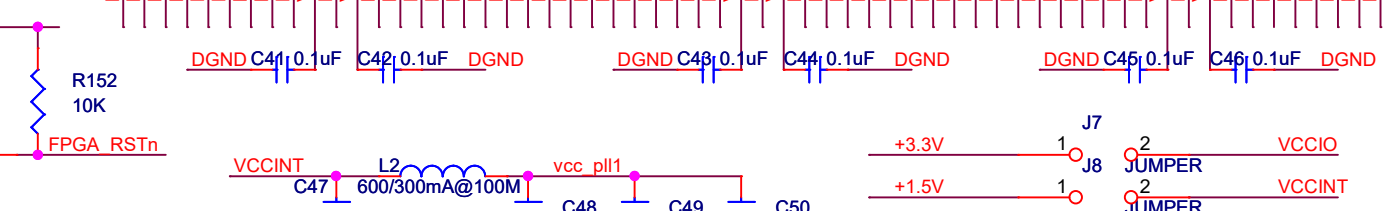
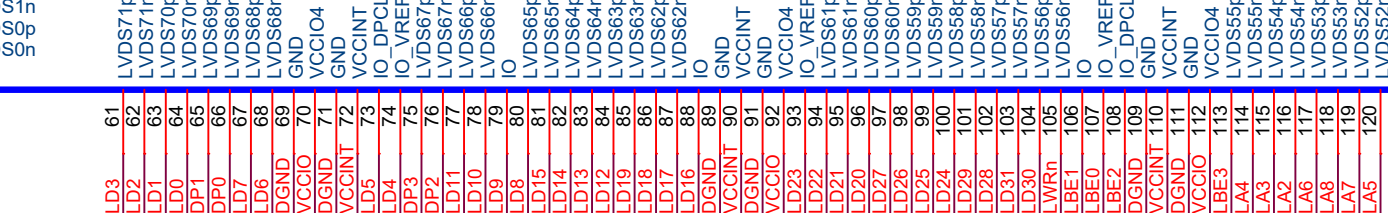
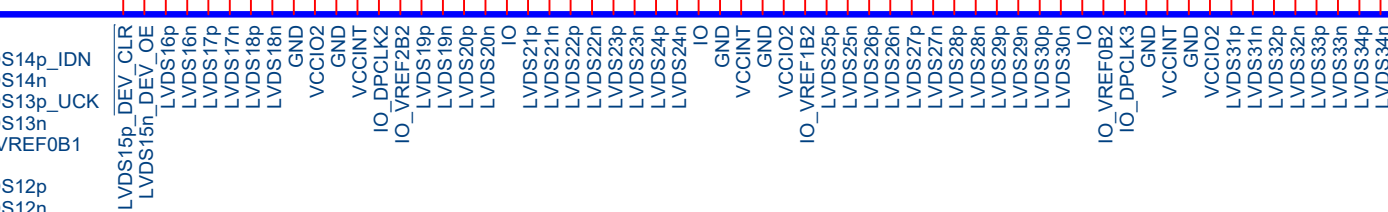
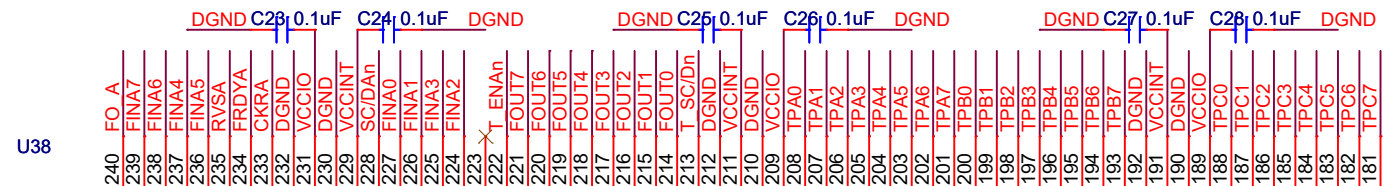
**! Inconsistent assignment  
Been corrected in FPGA pin assignment**



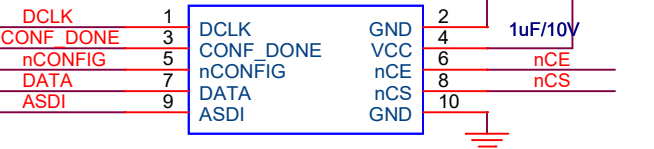
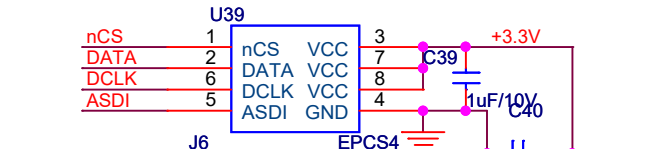
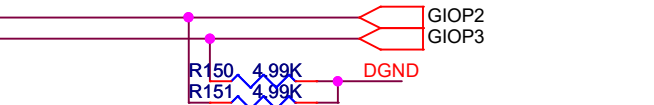
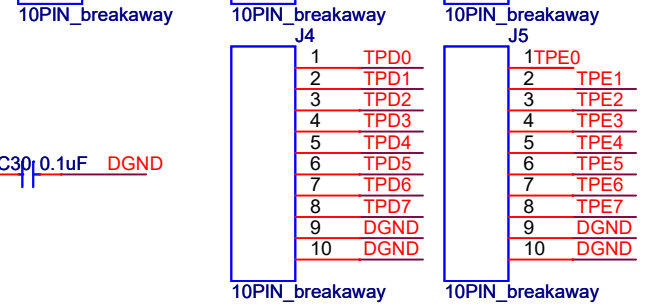
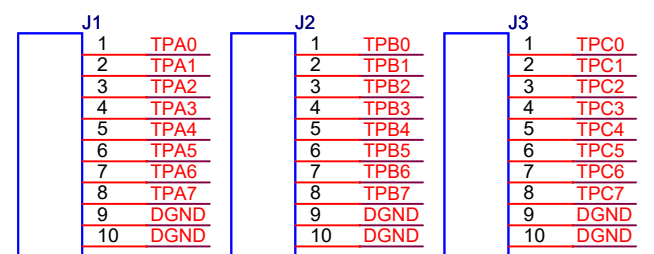
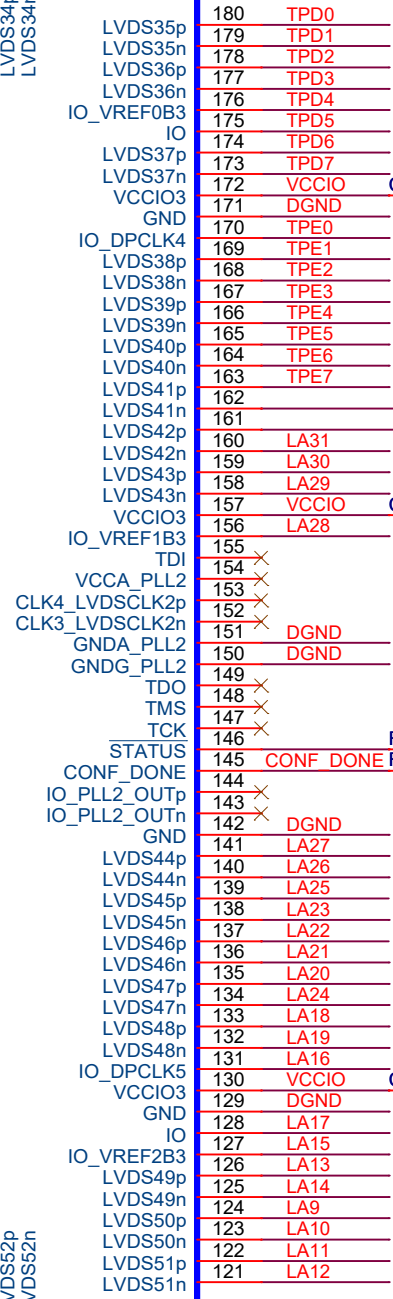
Title: <b>Optical Fiber Transceiver</b>		
Document Name: <b>Fiber Transceiver.sch</b>		Rev.: 1B
Designed By: <b>Yaoting</b>	Checked By: <b>Bob</b>	
Size: <b>B</b>	Updated: <b>Thursday, January 30, 2020</b>	Sheet: <b>3 of 5</b>



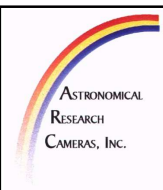
SW SPDT-8121SHAV2GE  
Msr: 611-8121SHAV2GE



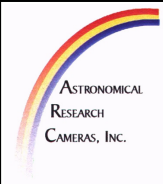
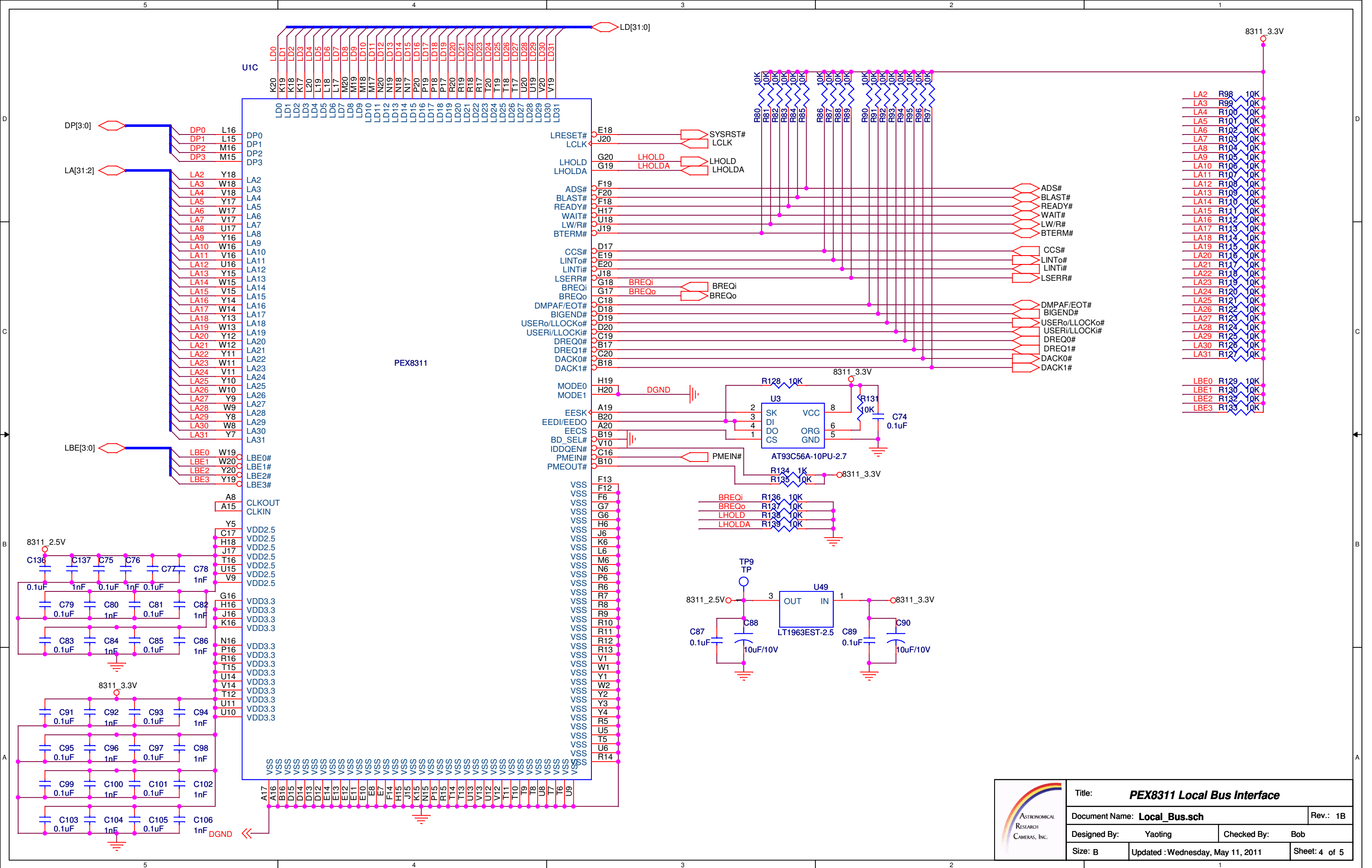
### EP1C6Q240C6



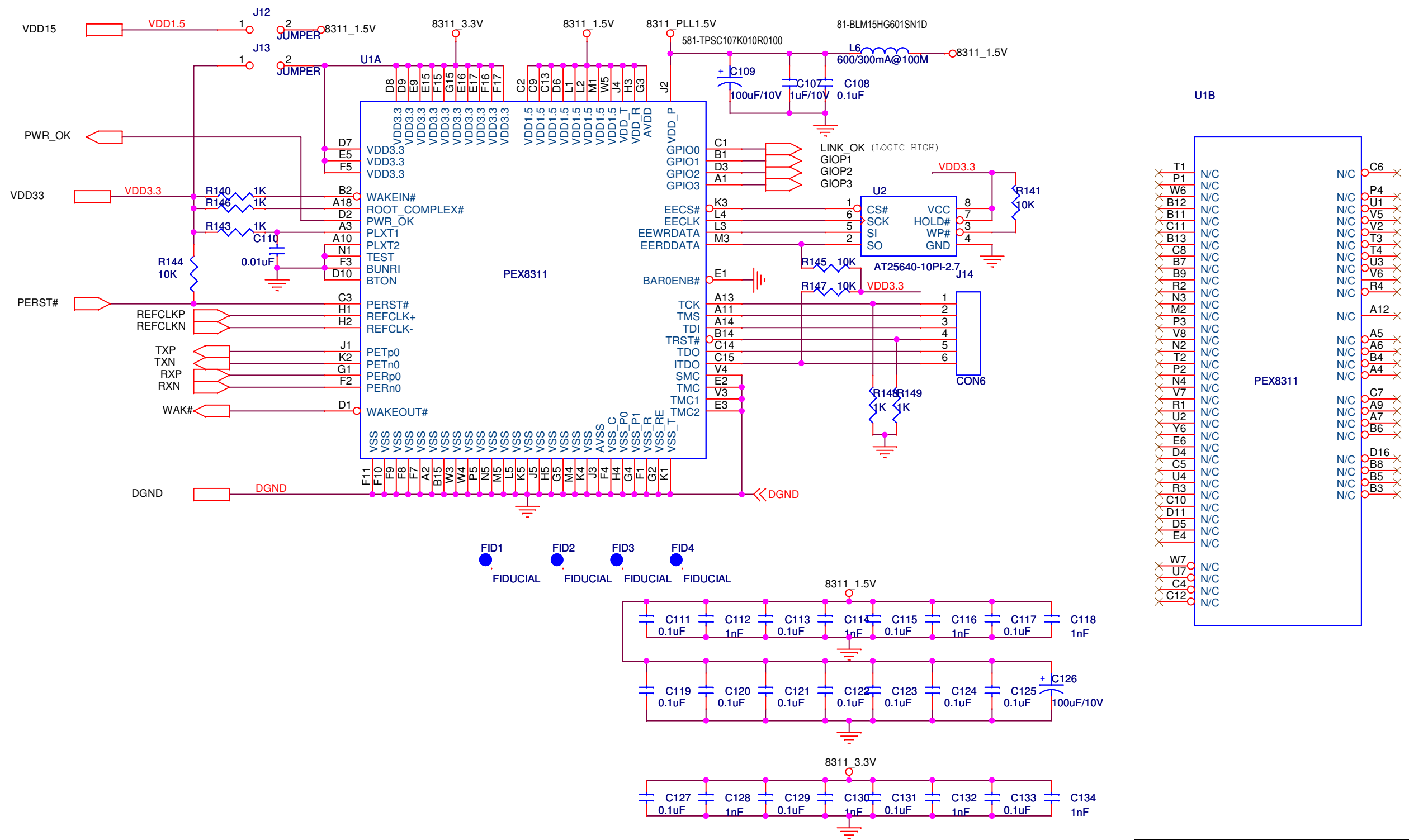
### ByteBlaster II



Title: <b>FPGA</b>		Rev.: 1B
Document Name: <b>FPGA_SCH.sch</b>		
Designed By: <b>Yaoting</b>	Checked By: <b>Bob</b>	
Size: <b>B</b>	Updated: <b>Thursday, January 30, 2020</b>	Sheet: <b>2 of 5</b>



Title: <b>PEX8311 Local Bus Interface</b>		
Document Name: <b>Local_Bus.sch</b>		Rev.: 1B
Designed By: <b>Yaoting</b>	Checked By: <b>Bob</b>	
Size: B	Updated: <b>Wednesday, May 11, 2011</b>	Sheet: 4 of 5



	Title: <b>PEX8311 PCIe Interface</b>		
	Document Name: <b>PIPE.SCH</b>		Rev.: <b>1B</b>
	Designed By: <b>Yaoting</b>	Checked By: <b>Bob</b>	
	Size: <b>B</b>	Updated: <b>Wednesday, May 11, 2011</b>	Sheet: <b>5 of 5</b>