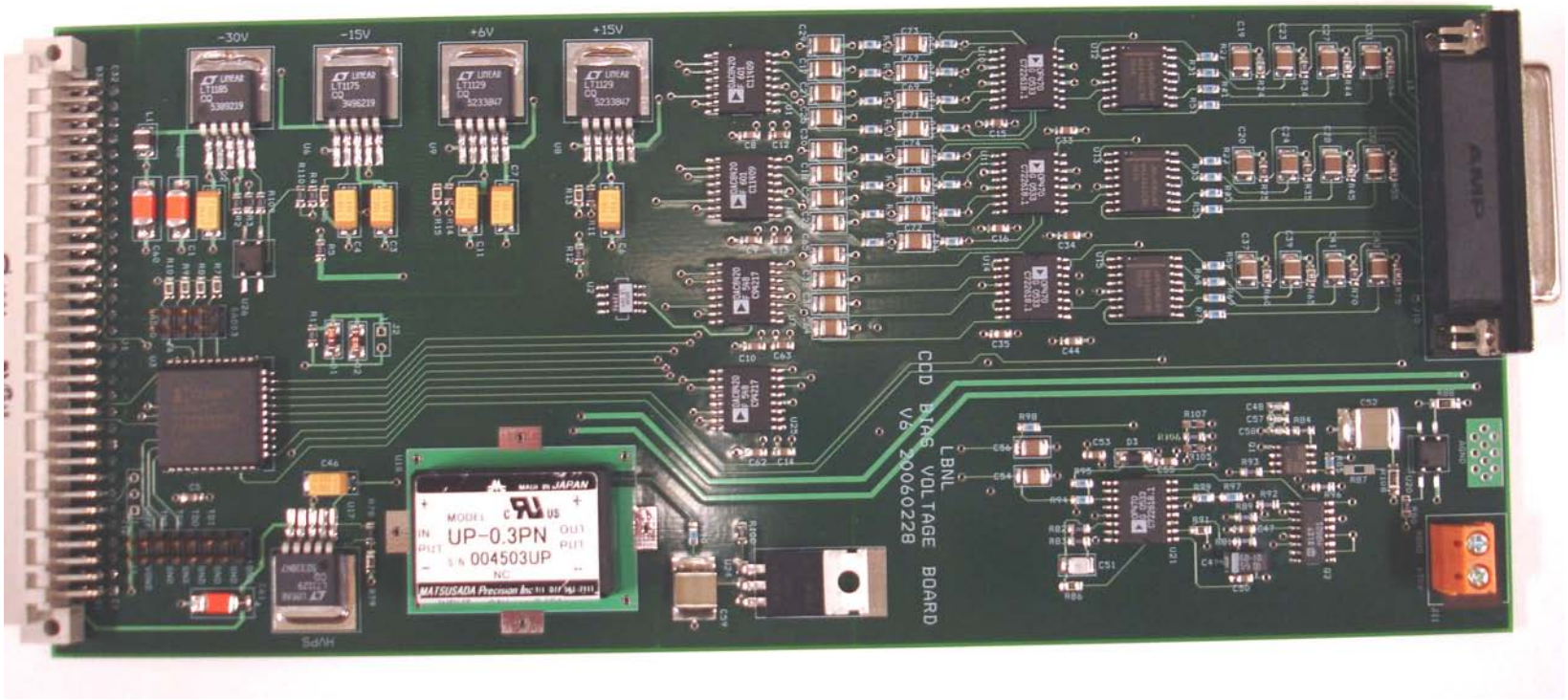
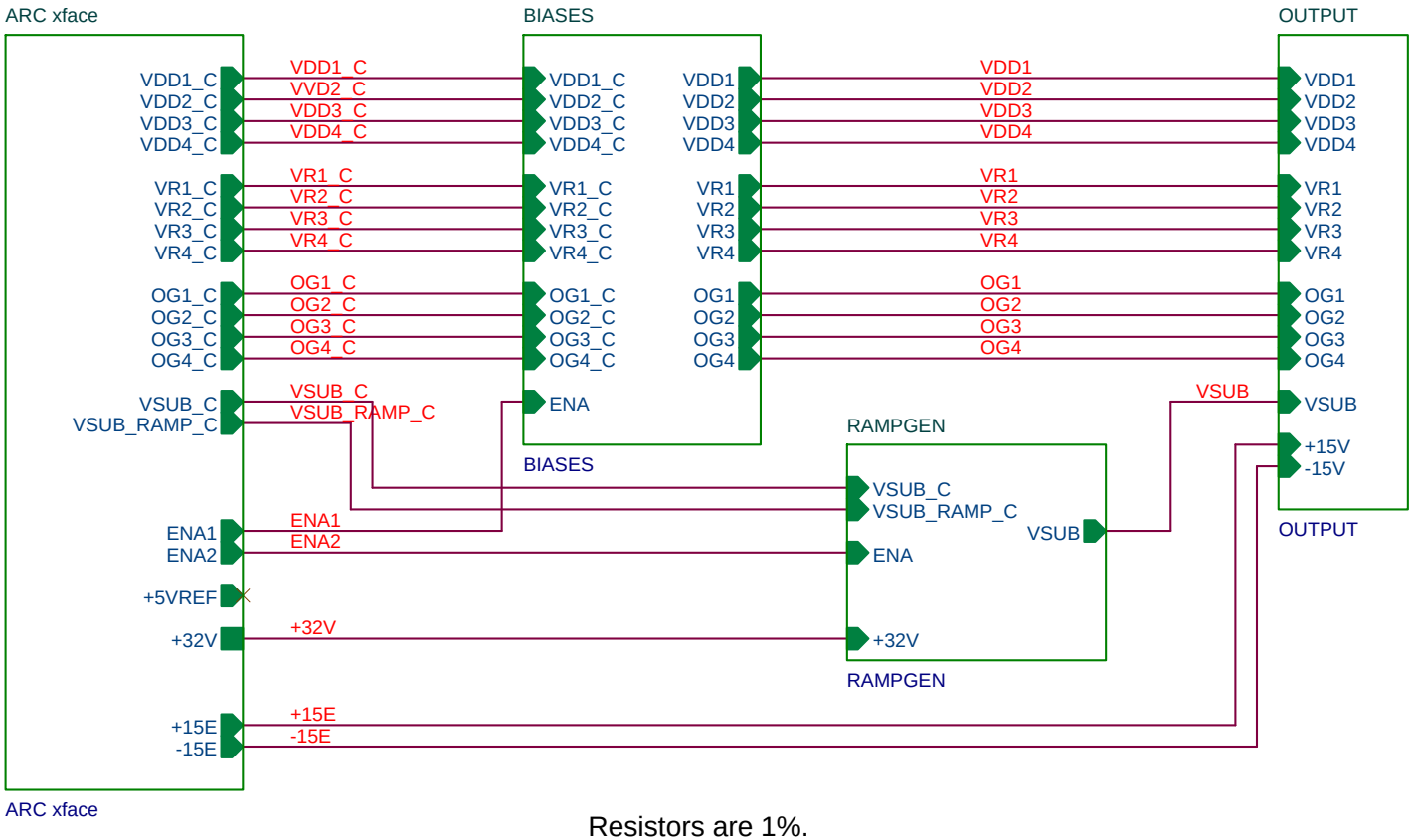

-30V
-15V
+6V
+15V
MADE IN JAPAN
MODEL
UP-0.3PN
S/N 004503UP
MATSUSADA Precision Inc
LBNL
CCD BIAS VOLTAGE BOARD
V6 20060228


UP-0.3PN
INPUT -24V 0.18A
LBNL
CCD BIAS VOLTAGE BOARD
V6 20060228




Resistors are 1%.

| | | | |
|---|---|---|---|
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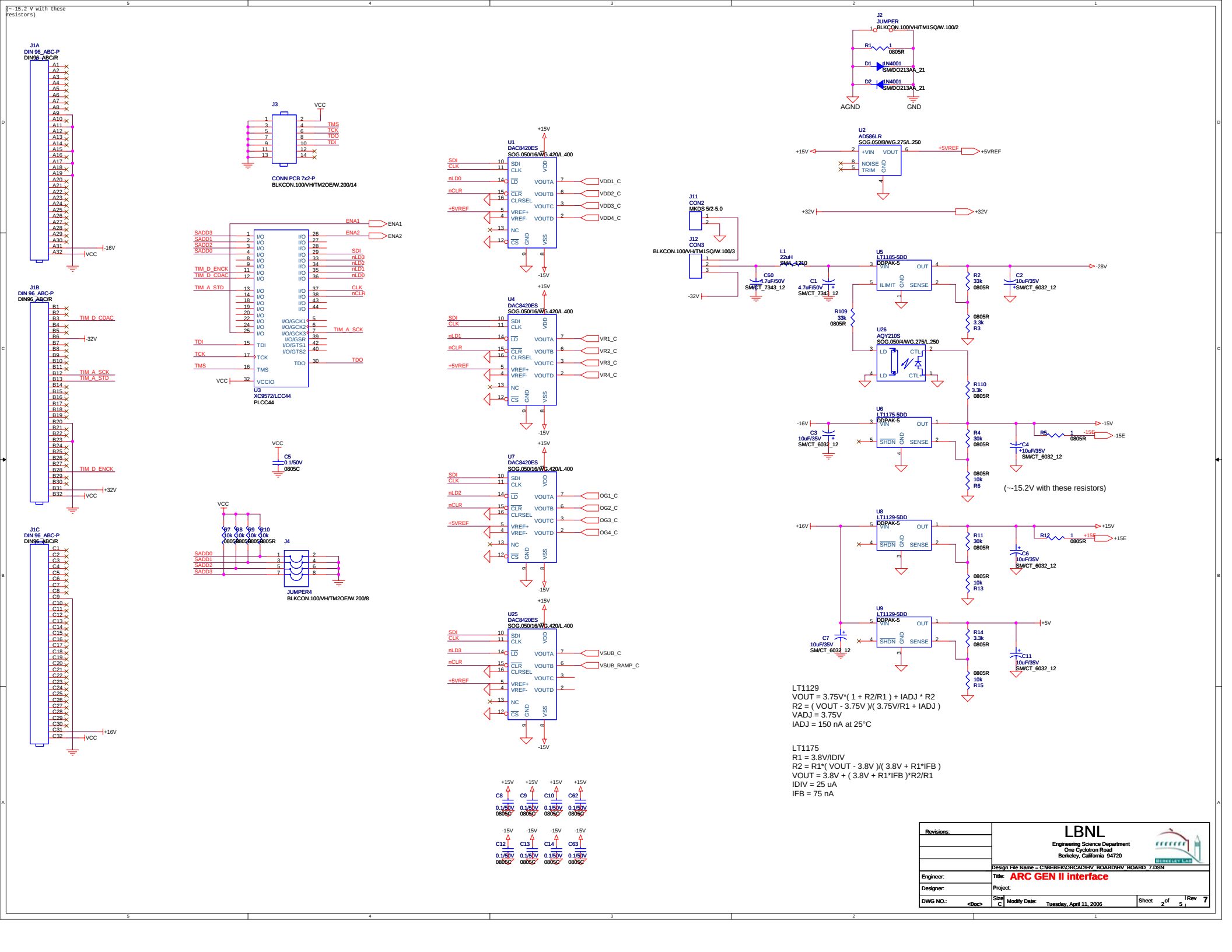
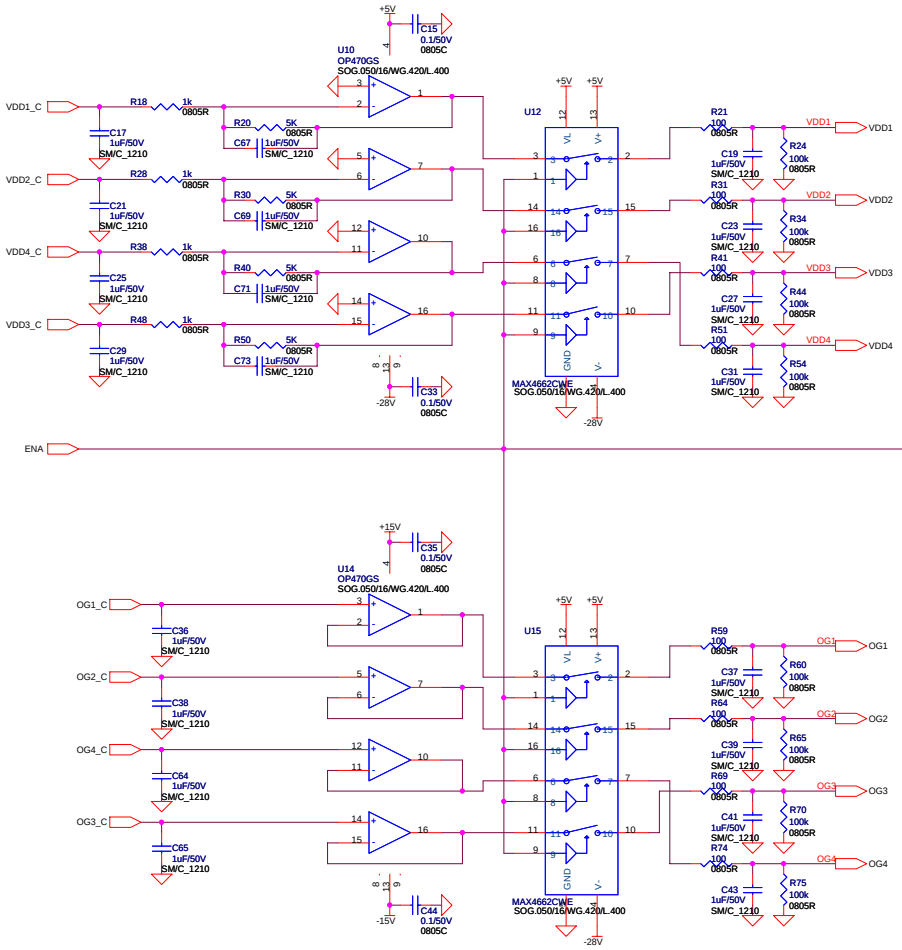
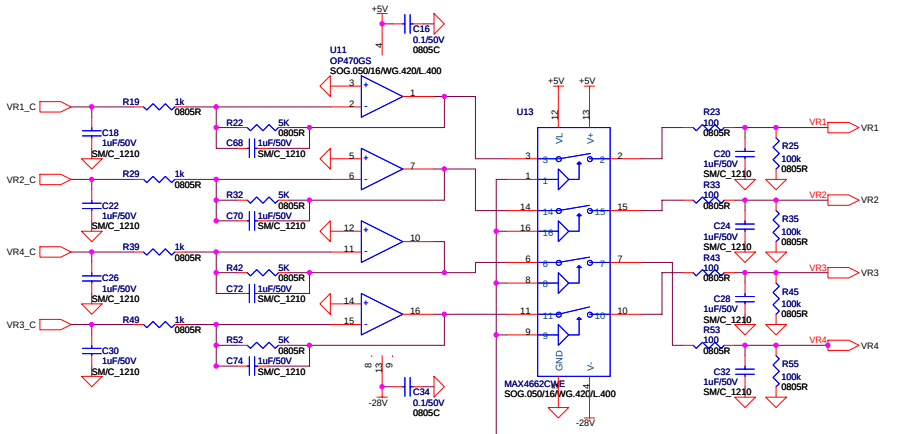
| | Design File Name = C:\BEBEK\ORCAD\HV_BOARD\HV_BOARD_7.DSN | | |
| Engineer: | Title: **CCD bias and substrate voltage generator** | | |
| Designer: | Project: | | |
| DWG NO.: <Doc> | Size C | Modify Date: Tuesday, April 11, 2006 | Sheet 1 of 5 / Rev 7 |


(~-15.2 V with these resistors)
J1A
DIN 96_ABC-P
DIN96_ABC/R
-16V
VCC
J1B
DIN 96_ABC-P
DIN96_ABC/R
TIM_D_CDAC
-32V
TIM_A_SCK
TIM_A_STD
TIM_D_ENCK
+32V
VCC
J1C
DIN 96_ABC-P
DIN96_ABC/R
+16V
VCC
J3
VCC
TMS
TCK
TDO
TDI
CONN PCB 7x2-P
BLKCON.100/VH/TM2OE/W.200/14
ENA1
ENA2
SADD3
SADD1
SADD2
SADD0
SDI
nLD3
nLD2
nLD1
nLD0
TIM_D_ENCK
TIM_D_CDAC
TIM_A_STD
CLK
nCLR
TIM_A_SCK
TDI
TCK
TMS
TDO
VCC
U3
XC9572/LCC44
PLCC44
VCC
C5
0.1/50V
0805C
VCC
R7 10k 0805R
R8 10k 0805R
R9 10k 0805R
R10 10k 0805R
SADD0
SADD1
SADD2
SADD3
J4
JUMPER4
BLKCON.100/VH/TM2OE/W.200/8
+15V
U1
DAC8420ES
SOG.050/16/WG.420/L.400
SDI
CLK
nLD0
nCLR
+5VREF
VDD1_C
VDD2_C
VDD3_C
VDD4_C
-15V
U4
DAC8420ES
SOG.050/16/WG.420/L.400
nLD1
VR1_C
VR2_C
VR3_C
VR4_C
U7
DAC8420ES
SOG.050/16/WG.420/L.400
nLD2
OG1_C
OG2_C
OG3_C
OG4_C
U25
DAC8420ES
SOG.050/16/WG.420/L.400
nLD3
VSUB_C
VSUB_RAMP_C
C8 C9 C10 C62
C12 C13 C14 C63
0.1/50V
0805C
J2
JUMPER
BLKCON.100/VH/TM1SQ/W.100/2
R1 1 0805R
D1 1N4001 SM/DO213AA_21
D2 1N4001 SM/DO213AA_21
AGND
GND
U2
AD586LR
SOG.050/8/WG.275/L.250
+VIN
VOUT
NOISE
TRIM
+5VREF
+32V
J11
CON2
MKDS 5/2-5.0
J12
CON3
BLKCON.100/VH/TM1SQ/W.100/3
-32V
L1
22uH
SMA_1210
C60
4.7uF/50V
SM/CT_7343_12
C1
4.7uF/50V
SM/CT_7343_12
U5
LT1185-SDD
DDPAK-5
VIN
OUT
ILIMIT
GND
SENSE
-28V
R2
33k
0805R
R3
3.3k
0805R
C2
10uF/35V
SM/CT_6032_12
R109
33k
0805R
U26
AQV210S
SOG.050/4/WG.275/L.250
LD
CTL
R110
3.3k
0805R
U6
LT1175-SDD
DDPAK-5
SHDN
-16V
C3
10uF/35V
SM/CT_6032_12
R4
30k
0805R
R5 1 -15E 0805R
C4
+10uF/35V
SM/CT_6032_12
R6
10k
0805R
(~-15.2V with these resistors)
U8
LT1129-SDD
DDPAK-5
+16V
R11
30k
0805R
R12 1 +15E 0805R
C6
10uF/35V
SM/CT_6032_12
R13
10k
0805R
U9
LT1129-SDD
DDPAK-5
C7
10uF/35V
SM/CT_6032_12
R14
3.3k
0805R
+5V
C11
10uF/35V
SM/CT_6032_12
R15
10k
0805R
LT1129
VOUT = 3.75V*( 1 + R2/R1 ) + IADJ * R2
R2 = ( VOUT - 3.75V )/( 3.75V/R1 + IADJ )
VADJ = 3.75V
IADJ = 150 nA at 25°C
LT1175
R1 = 3.8V/IDIV
R2 = R1*( VOUT - 3.8V )/( 3.8V + R1*IFB )
VOUT = 3.8V + ( 3.8V + R1*IFB )*R2/R1
IDIV = 25 uA
IFB = 75 nA
Revisions:
LBNL
Engineering Science Department
One Cyclotron Road
Berkeley, California 94720
Design File Name = C:\BEBEK\ORCAD\HV_BOARD\HV_BOARD_7.DSN
Engineer:
Title: ARC GEN II interface
Designer:
Project:
DWG NO.: <Doc>
Size: C
Modify Date: Tuesday, April 11, 2006
Sheet 2 of 5
Rev 7

DAC IN 0 - +5V gives 0 - -25V

DAC IN 0 - +5V gives 0 - -25V




DAC IN 0 - +5V gives 0 - +5V

| | |
|---|---|
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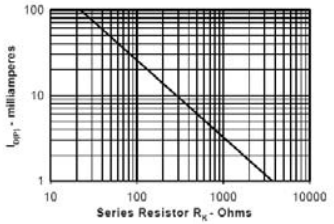
| | Design File Name = C:\BEBEK\ORCAD\HV_BOARD\HV_BOARD_7.DSN |
| Engineer: | Title: **Bias drivers** |
| Designer: | Project: **<Project>** |
| DWG NO.: <Doc> | Size: C \| Modify Date: Tuesday, April 11, 2006 \| Sheet 3 of 5 \| Rev 7 |

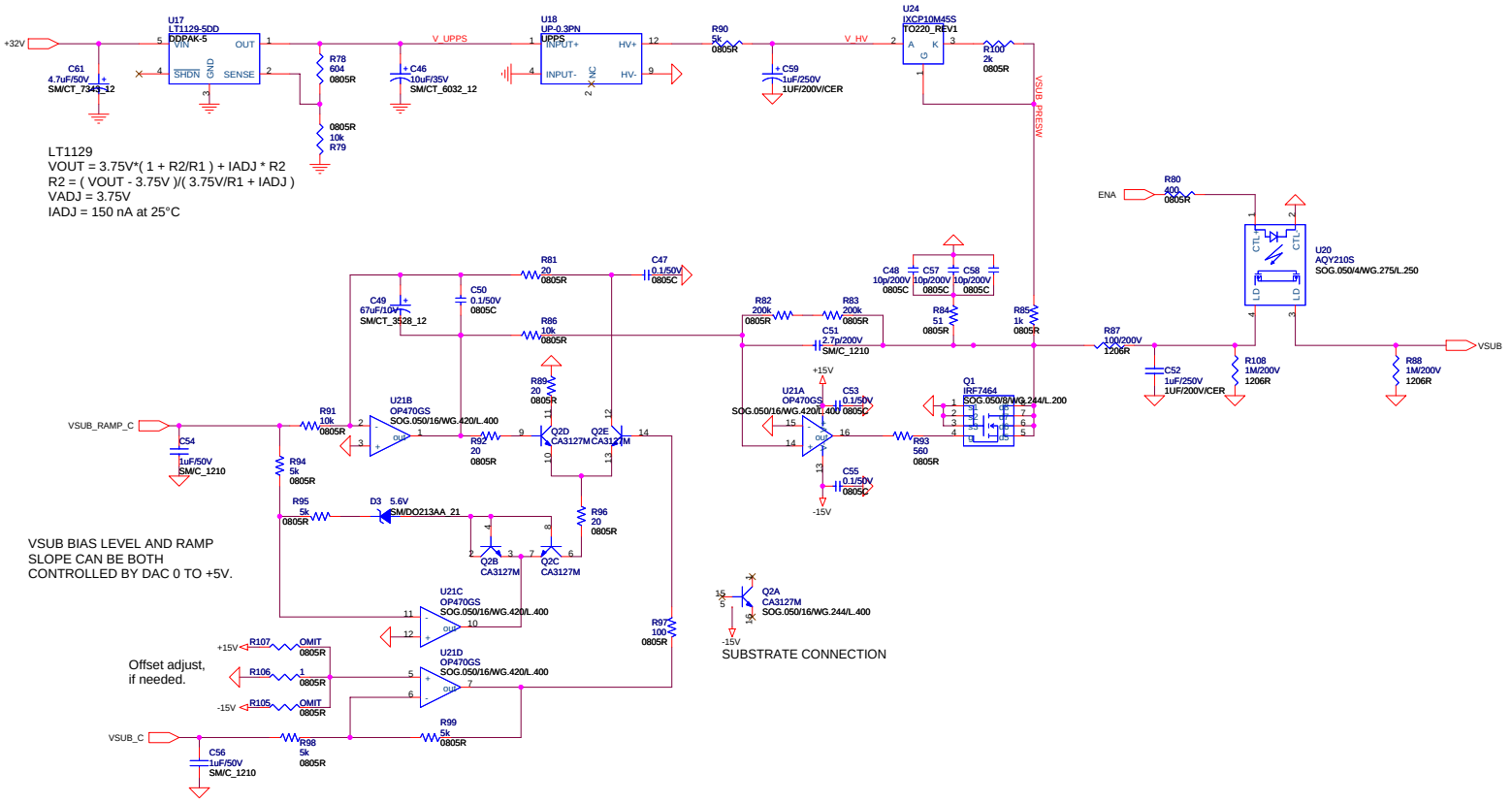
For UP-0.3 power supply R78 =
604 for 4V for 50V
11.3k for 8V for 100V
33.0k for 16V for 200V

For UP-0.1 power supply R78 =
53.6k for 24V for 100V
22.1k for 12V for 50V

Matsusada
UP-0.3 300V supply or
UP-0.1 100V supply
0-24V input 0 to full scale




2 mA currrent limiter.

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|---|---|
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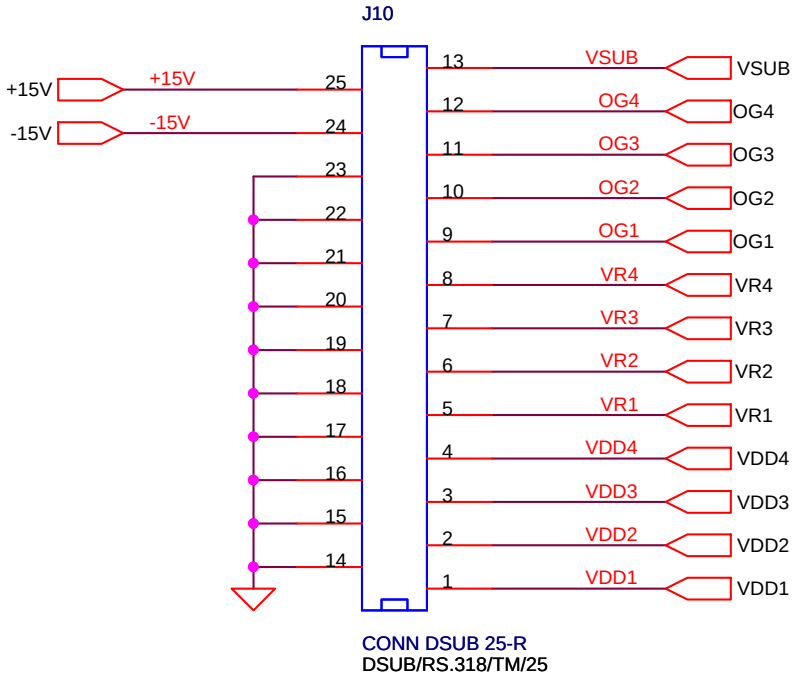
| | Design File Name = C:\BEBEK\ORCAD\HV_BOARD\HV_BOARD_7.DSN |
| Engineer: | Title: CCD ERASE RAMP GENERATOR 8 |
| Designer: | Project: |
| DWG NO.: <Doc> | Size: C Modify Date: Tuesday, April 11, 2006 Sheet 5 of 5 Rev 7 |




| | |
|---|---|
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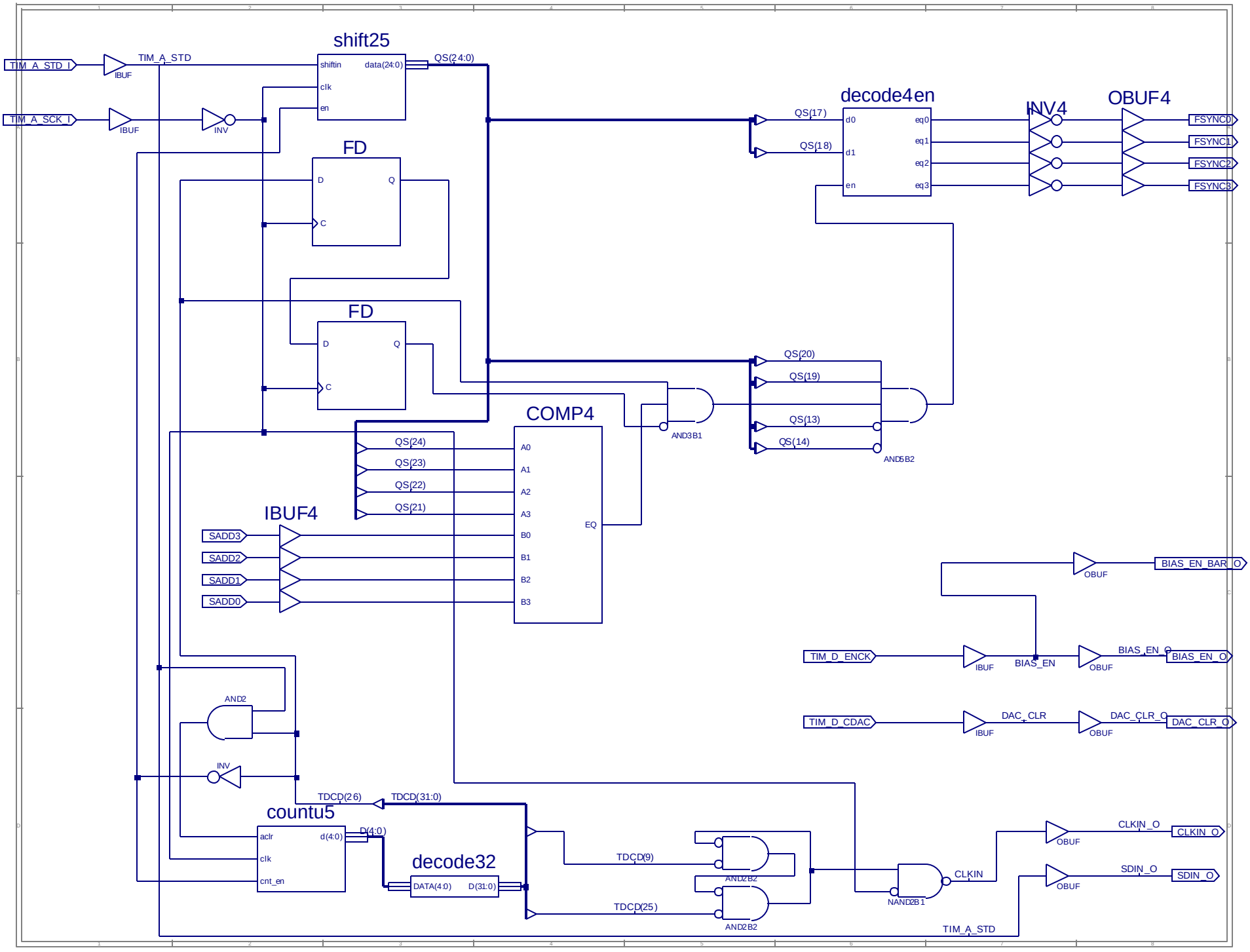
| | C:\BEBEK\ORCAD\HV_BOARD\HV_BOARD_7.DSN |
| Engineer: **<Engineer>** | Title: **Output connector** |
| Designer: **<Designer>** | Project: **<Project>** |
| DWG NO.: **<Doc>** | Size: <Drawing Size> Modify Date: Tuesday, April 11, 2006 Sheet 4 of 5 Rev 7 |


shift25
TIM_A_STD_I
IBUF
TIM_A_STD
shiftin
data(24:0)
QS(24:0)
clk
en
TIM_A_SCK_I
IBUF
INV
FD
D
Q
C
FD
D
Q
C
decode4en
QS(17)
QS(18)
d0
d1
en
eq0
eq1
eq2
eq3
INV4
OBUF4
FSYNC0
FSYNC1
FSYNC2
FSYNC3
QS(20)
QS(19)
QS(13)
QS(14)
AND3B1
AND5B2
COMP4
QS(24)
QS(23)
QS(22)
QS(21)
A0
A1
A2
A3
B0
B1
B2
B3
EQ
IBUF4
SADD3
SADD2
SADD1
SADD0
OBUF
BIAS_EN_BAR_O
TIM_D_ENCK
IBUF
BIAS_EN
OBUF
BIAS_EN_O
BIAS_EN_O
TIM_D_CDAC
IBUF
DAC_CLR
OBUF
DAC_CLR_O
DAC_CLR_O
AND2
INV
TDCD(26)
TDCD(31:0)
countu5
aclr
clk
cnt_en
d(4:0)
D(4:0)
decode32
DATA(4:0)
D(31:0)
TDCD(9)
TDCD(25)
AND2B2
AND2B2
NAND2B1
CLKIN
OBUF
CLKIN_O
CLKIN_O
SDIN_O
OBUF
SDIN_O
TIM_A_STD