ARC-32: CCD & IR Clock Driver Board

The clock driver board translates digital input signals into analog output signals for direct connection to CCD and infrared arrays. It provides 24 clock signals, each of which has programmable high and low voltages. Their rise and fall times can be adjusted by inserting resistors and capacitors in the output circuit. This board is set up to drive up to +/- 13 volts for operating CCD arrays, or much lower unipolar voltages for operating IR arrays. It is similar in function to two earlier products, the CCD clock driver (ARC30) and IR clock driver (ARC31), but is intended to be used for both CCD and IR arrays.

OPERATION

The logical state of each of the clock drivers is controlled by the Switch State bits SS15-SS0, generated by the timing board. The timing board writes its DSP data bits D15-D0 to the backplane as SS15-SS0 whenever the DSP writes to the switch state memory mapped address ($FFB0 for Gen II and $FFFFF3 for Gen III), valid on the rising edge of the strobe signal WRSS. The remaining data bits D23-D16 are used as inputs to the delay counter on the timing board. The addressing lines SS15-SS12 are input a PAL on the clock driver board to act as board and bank select lines. The data lines SS11 to SS0 are latched into the PAL if the address lines SS15-SS13 match the state of the board address jumpers JP12 to JP10.

The address line SS12 selects to update either the lower bank of the clock driver signals CLK 11 to CLK0 (SS12 = 0) or the upper bank CLK23 to CLK12 (SS12 = 1), allowing twelve of the twenty-four clock signals to be changed in a single timing board instruction. Alternatively, the control line TIM-D-AUX can be set high to cause the lower and upper clock driver banks to update simultaneously to the same switch state values on a single instruction, which may be useful for controlling mosaics that require twelve or fewer clocks per sensor. This is implemented in software as

```
DUALCLK   EQU   1                          ; Update both clock driver banks
          BSET  #DUALCLK,X:<LATCH          ; Change the software LATCH bit
          MOVEP X:LATCH,Y:WRLATCH          ; Write it value to the hardware
```

There is a provision for the user to display two selected clock driver outputs on an oscilloscope through the two SMB (push-on) coaxial connectors mounted next to the DB-37 output connector. They are connected to a set of six multiplexers that sample the clock driver outputs at the output connectors. Selection of any two outputs is made from the timing board with the "Set MultipleXer" command, located in either the "timCCDmisc.asm" or "timIRmisc.asm" file:

```
SMX  #clk_board  #MUX1  #MUX2
       #clk_board = 0 to 15 to select the desired clock driver board
       #MUX1 = 0 to 23 to select which clock driver output goes to the first SMB
       #MUX2 = 0 to 23 to select which clock driver output goes to the second SMB
```

There is a provision for connecting zener protection diodes from each output to ground. Zener protection diodes are routinely installed on IR boards since bipolar voltages often

cause latchup on their readout circuitry.

JUMPERS and CUSTOMIZATIONS

The board addressing jumpers are located next to the PAL near the backplane connector. The state of the clock outputs follows the data bits D11-D0 when the data bits D19-D17 match the jumpers 0, 1 and 2 installed in the header marked SWITCH on the board. Notice that the data bit D16 is used to select the high or low bank of 12 clocks on a board.

The high and low clock voltages are programmed into a set of 8-bit Maxim MAX529 digital-to-analog converters, using the timing board DSP's synchronous serial link. This is done by calling the subroutine XMIT_A_WORD, located in the file "timboot.asm". The jumpers 0, 1, 2 and 3 near the DAC label are used for addressing which board will have its DACs written to. If these four jumpers match the values D23-D20 in the serial word then the appropriate DAC will be written to.

Up to eight separate clock driver boards with different SWITCH jumper settings may be installed in a single system. More than one clock driver board may be installed in the same controller with the same SWITCH jumper assignments, making the timing of their waveforms identical, but their high and low voltages different. Up to sixteen clock driver boards, each with different sets of clocking voltages and DAC jumper settings, may be installed in a single system.

Voltage selection jumpers can be set to make the clock drivers either unipolar positive, unipolar negative or bipolar. These are located in the middle top of the board, above the REFH and REFL labels. The jumper connects the DAC input reference pins either to a voltage reference or to ground. These are the jumper settings for the three useful cases -

	REFH	REFL
Bipolar	+	-
Unipolar negative	G	-
Unipolar positive	+	G

The maximum and minimum values attainable at the clock driver output pins are determined by the values of resistors R2, R102 and R103, located to the left of the jumpers that set the polarity of the reference voltages. CCD systems are generally configured to give +/- 13 volts range, whereas IR systems typically have unipolar swings of either +3.3 or +5.0 volts.

SOFTWARE DIFFERENCES with EARLIER BOARDS

The ARC32 uses different DACs from earlier boards, requiring a different serial data word to be constructed to update their output voltages. The software impact is seen in two places, as follows -

(1) The meanings of the bits in the 24-bit word that is sent serially to the DACs in the system have been changed because of a selection of 8 versus 12 bit DACs. The table in the waveforms file that writes these numbers to all the DACs in the system, usually

during the setup process, is quite different. For ARC32, the two lines neded for writing the high and low values to the first clock are

```
DC      $2A0080                                         ; DAC = unbuffered mode
DC      $200100+@CVI((RG_HI+Vmax)/(2*Vmax)*255)  ; Pin #1, RG Left
DC      $200200+@CVI((RG_LO+Vmax)/(2*Vmax)*255)
```

compared to the two lines for the ARC30 or ARC31 boards -

```
DC      (CLK2<<8)+(0<<14)+@CVI((RG_HI+10.0)/20.0*4095)    ; Pin #1,  RG
DC      (CLK2<<8)+(1<<14)+@CVI((RG_LO+10.0)/20.0*4095)
```

The sixteen most significant bits ($2001 and $2002) select the DAC and its internal register to write the least significant 8 bits to, and the @CVI with its argument is used to construct the 8-bit value to be written. The constants Vmax is separately defined in the file, and is nominally 13 for CCD boards. It is generally much less for boards configured to operate IR arrays. Additionaly, the first instruction of the table is needed to internally configure all the DACs in the system, and an eight bit value is generated by dividing by 255 rather than obtaining a 12 bit value by dividing by 4095.

(2) The "Set Bias Number" routine in either the "timCCDmisc.asm" or "timIRmisc.asm" file is different because of the change in DACs. Example code is available on request.

RELEASE NOTES

The current release of the ARC-32 clock driver board is Rev. 6A, dated 6/6/2006. It uses LM7171 op amp for the drivers. Compared to all earlier revisions of the clock driver board, including the ARC-30 and ARC-32, this board inverts the meaning of the jumpers in an attempt to use fewer of them. An installed jumper in this revision matches a "1" or a set bit in the address. The default settings for these jumpers is for board #2, whereby the DACs will get updated if the number 2 is the most significant nibble of the serial word, and the switches will be updated if there is either a 2 or a 3 in the board select nibble of the switch state word. These are the default settings for these two jumper blocks is:

DAC	0	1	2	3	SWITCH	0	1	2
	in	out	in	in		out	in	in

This is the opposite of earlier revisions Rev. 5A and 5B which require the inverse of these jumper placements.

A short description of the main differences between the three revisions of the board follows:

Rev. 5A – Utilizes the current feedback op amp THS3001, featuring high drive currents (120 mA), and fast rise times (~7nanosec).

Rev. 5B – Corrects the tendency of the THS3001 to thermally self-destruct if the clock driver outputs are shorted to ground by installing a 25 ohm series resistor in the output

and soldering the op amps to thermally conducting pads to conduct the heat away.

Rev. 6A – Settles for lower drive currents (100 mA versus 120 mA) and slower speed (20 nanosec versus 7 nanosec) in the interest of higher reliability and a cleaner output waveform due to the LM7171 op amp being a voltage feedback device. Reverses the sense of the addressing jumpers.

SPECIFICATIONS for Rev. 6A

Board Size	3.96 x 9.0 inches (3U width)
Number of channels	24 outputs available on a single male DB-37 connector
Drive capability	+/- 13 volts maximum 100 mA sustained current drive capability
Rise and fall times	User settable by installing resistors and capacitors with a default of 20 nanosec for a 10 volt change
Voltage resolution	The clock voltages are set with 8 bit DACs.
Diagnostic output	Any two clock driver outputs may be selected for viewing on SMB connectors