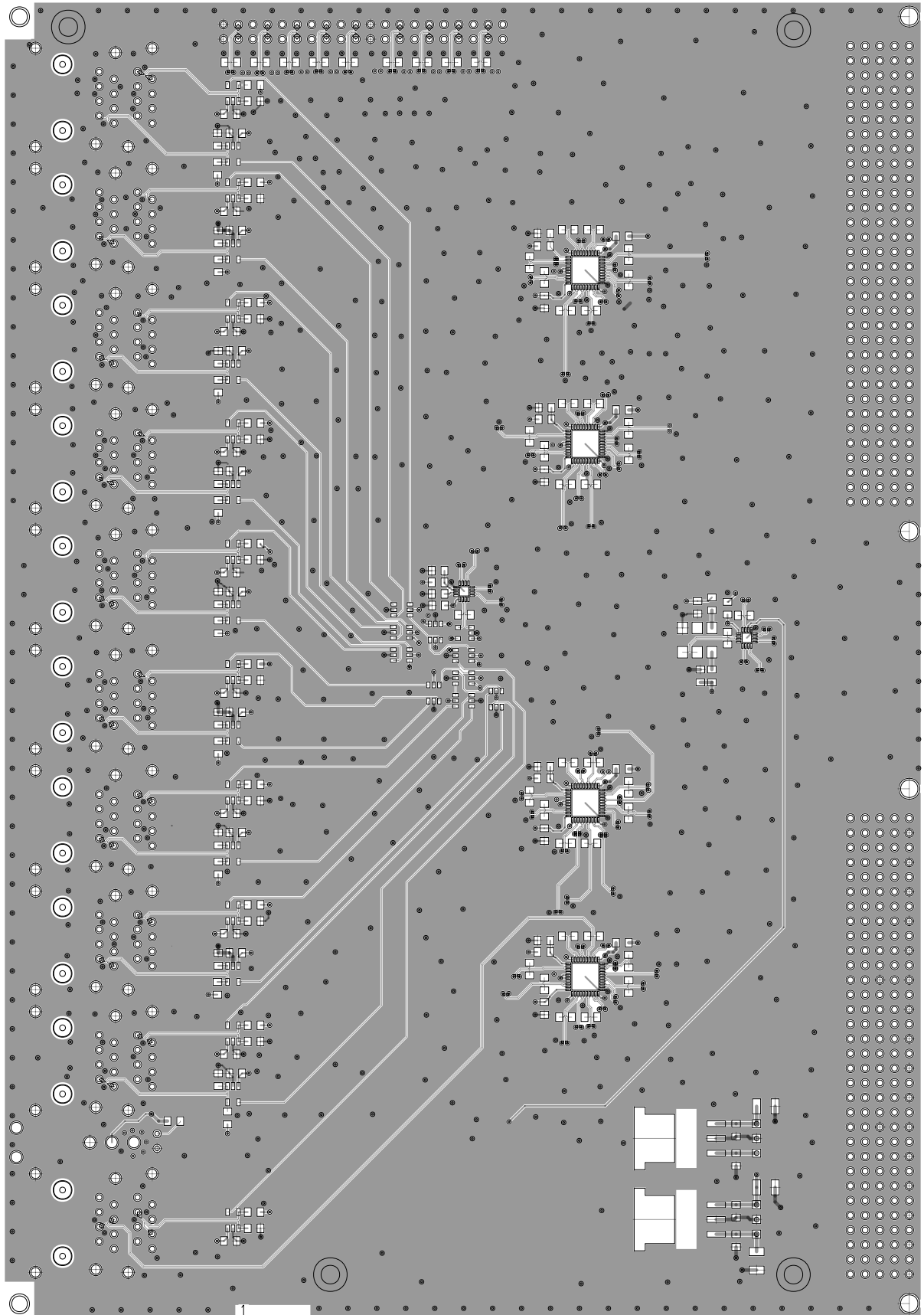
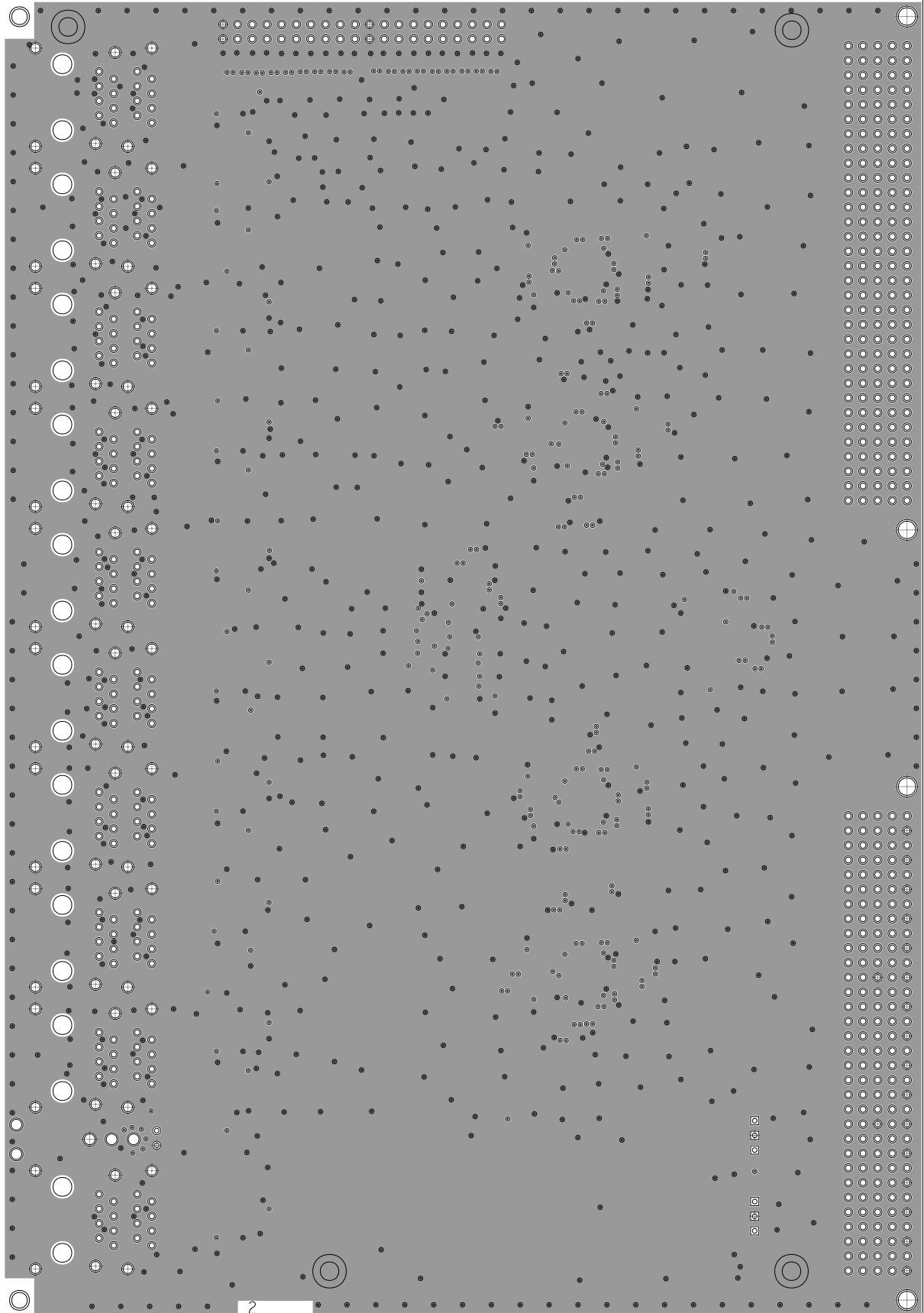


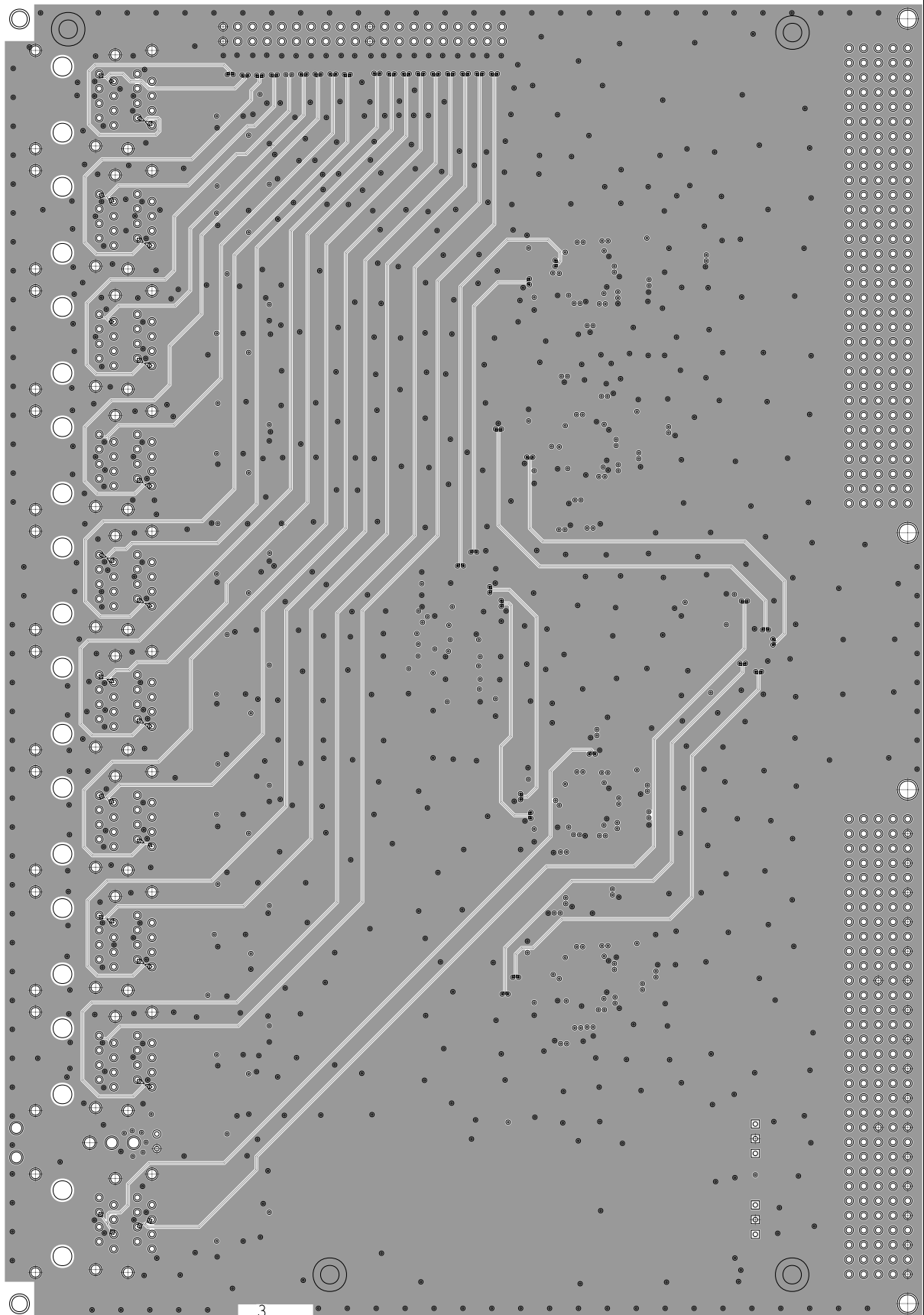
SYNC_BOARD_REVC_COTE_ELEMENTS



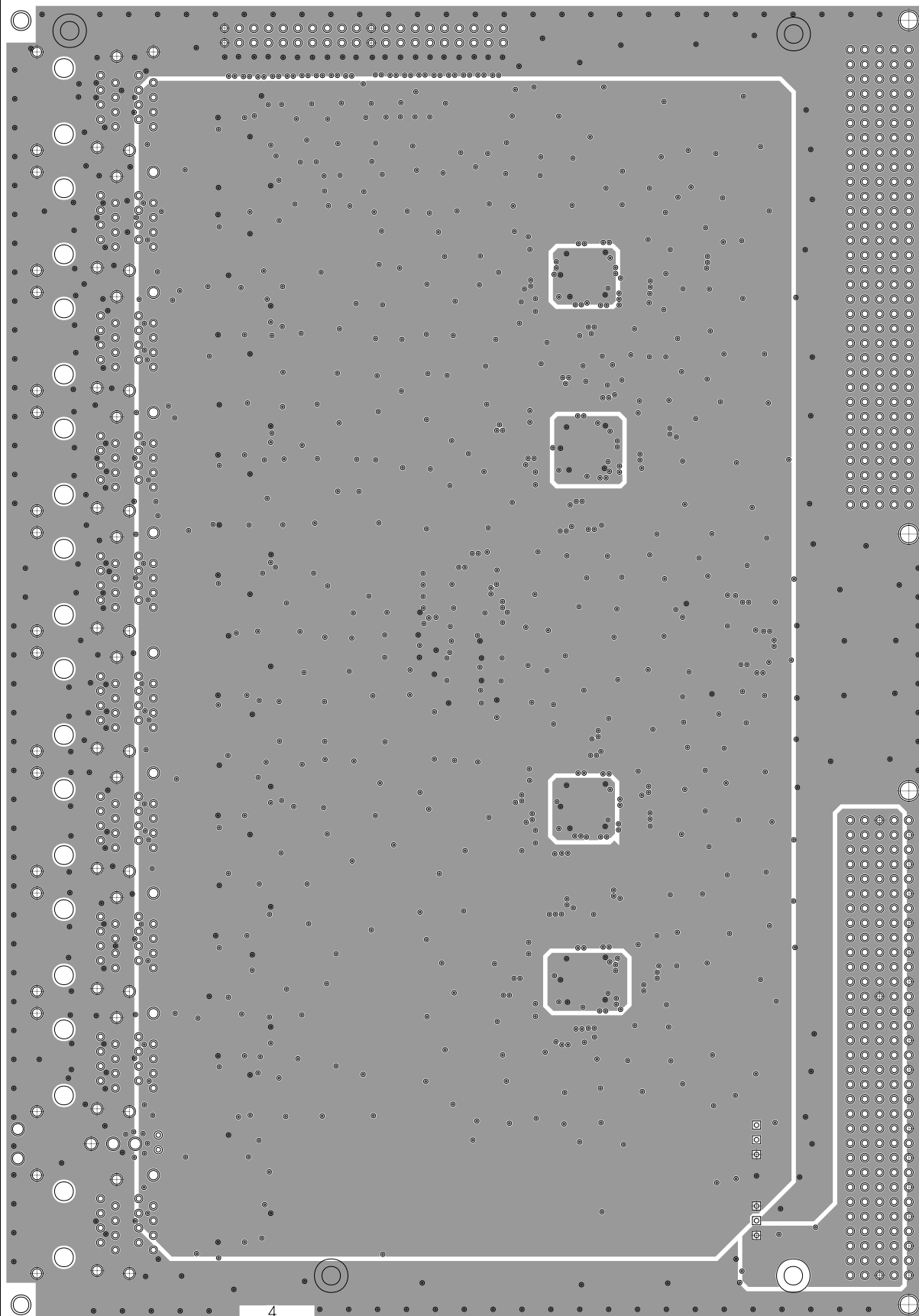
SYNC_BOARD_REVC_COUCHE_INTERNE 1



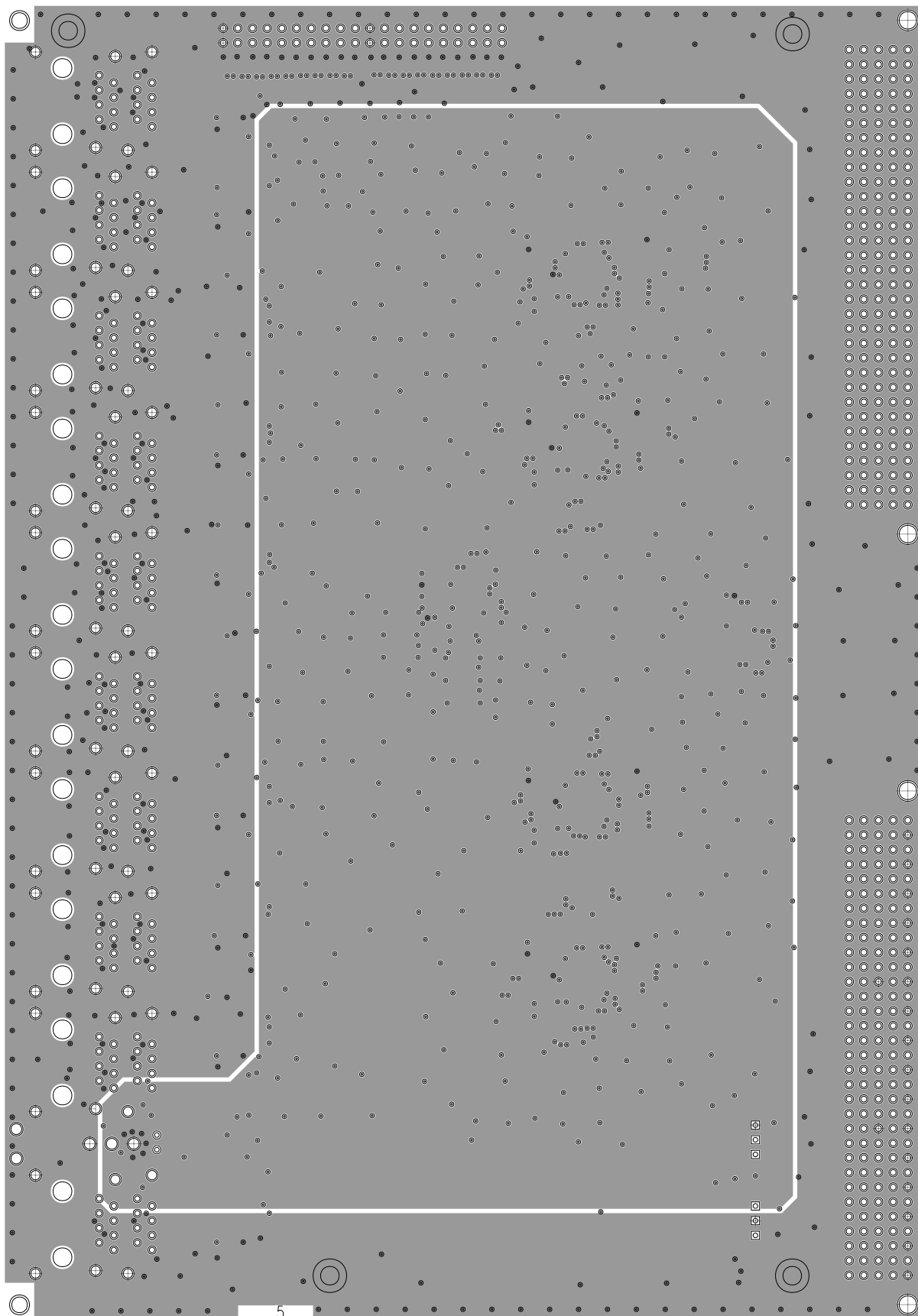
SYNC_BOARD_REVC_COUCHE_INTERNE2



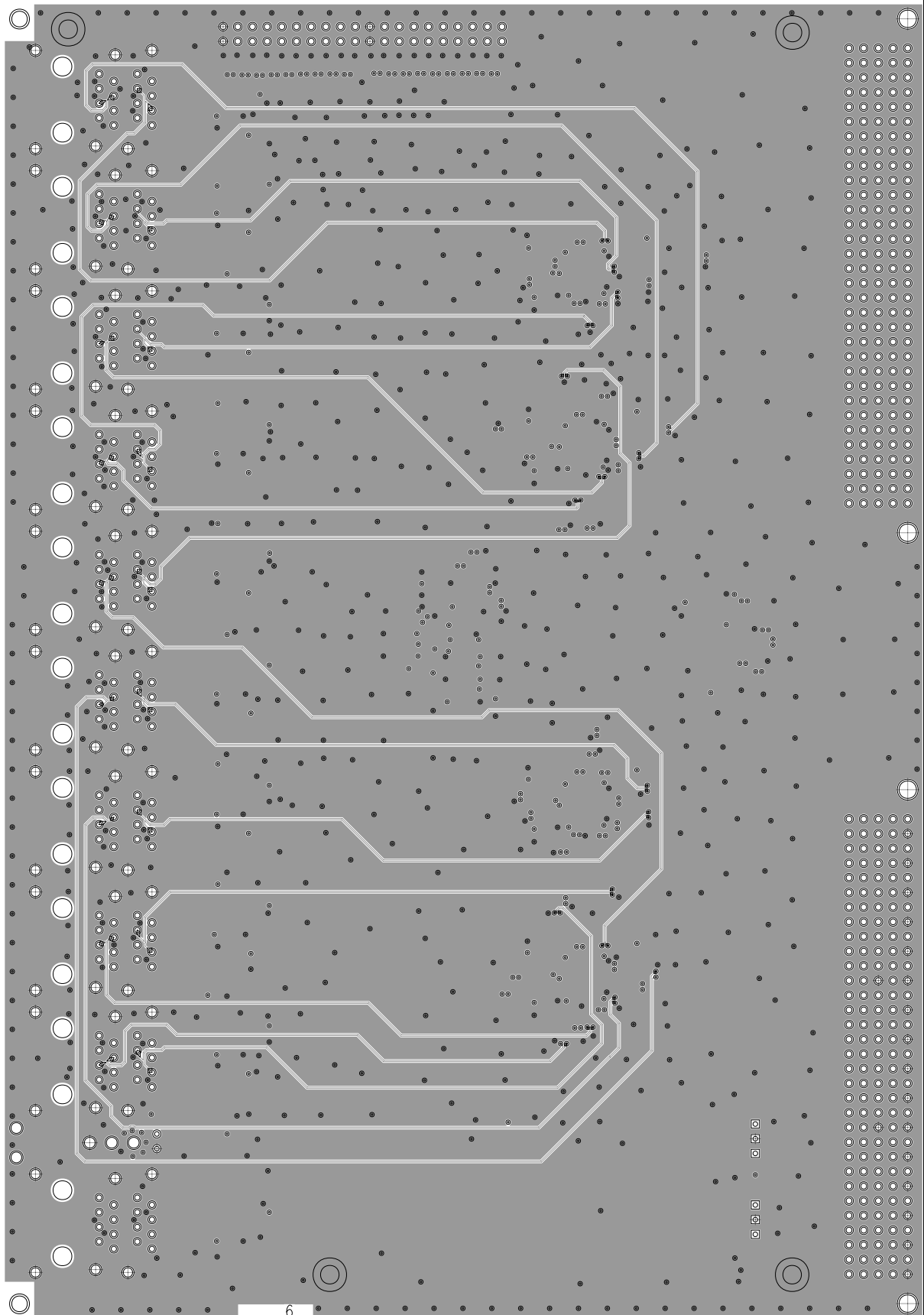
SYNC_BOARD_REVC_COUCHE_INTERNE3



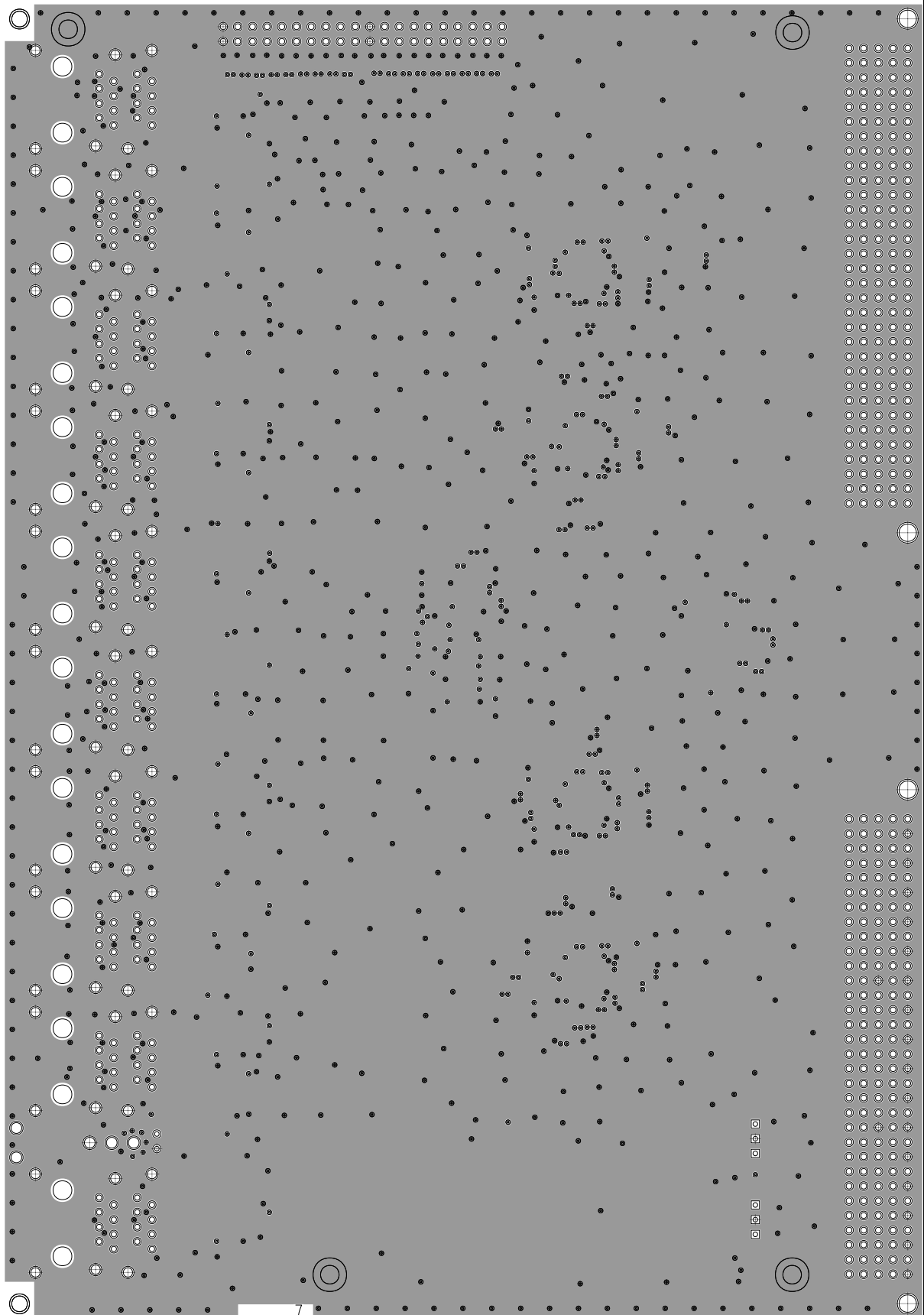
SYNC_BOARD_REVC_COUCHE_INTERNE4



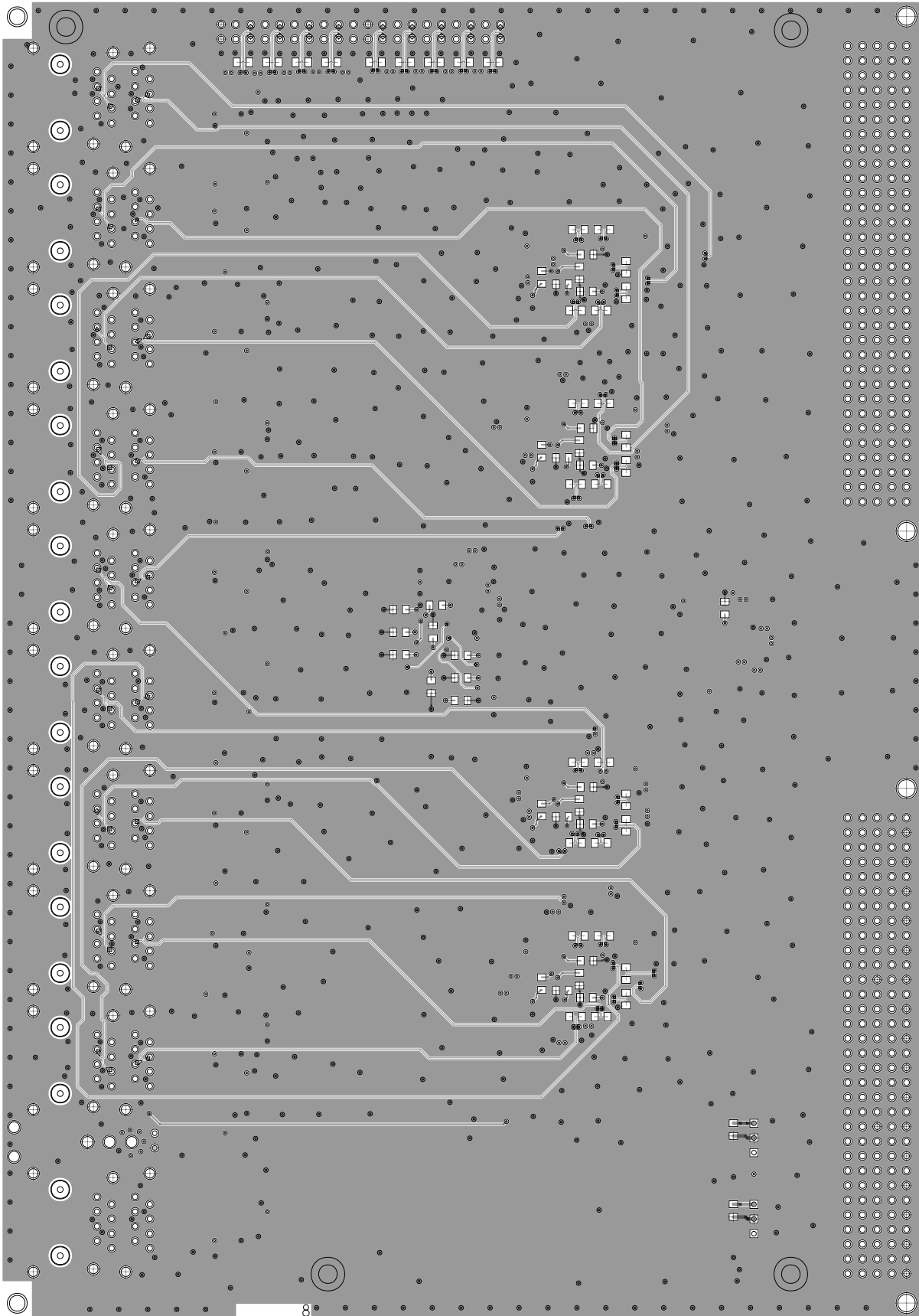
SYNC_BOARD_REVC_COUCHE_INTERNE5



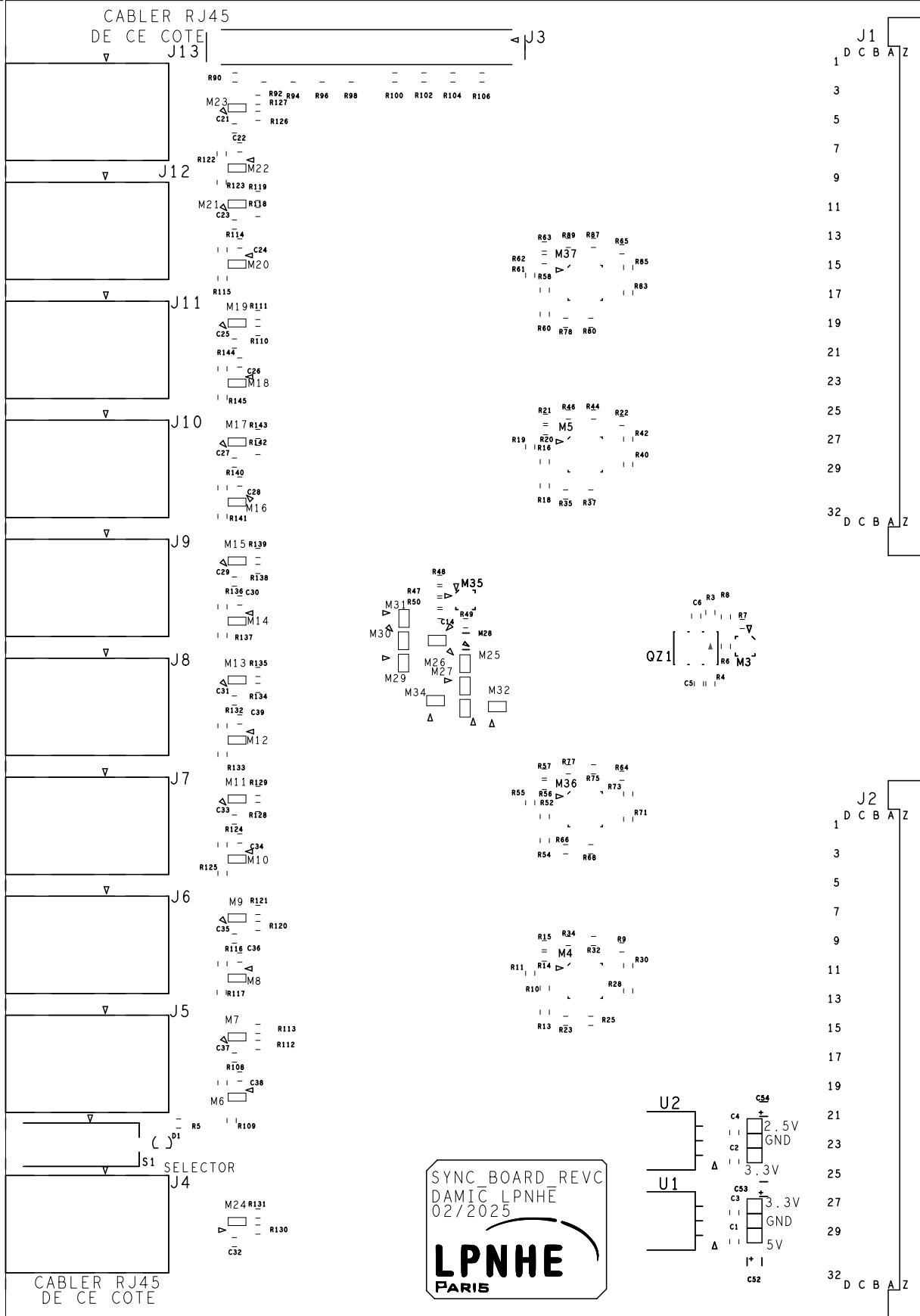
SYNC_BOARD_REVC_COUCHE_INTERNE6



2 SYNC_BOARD_REV_C_COTE_200DURE2



SYNC_BOARD_REVC_SERIGRAPHIE_ELEMENTS



—38	34	30	26	22	18	14	10	6	2
—	—	—	—	—	—	—	—	—	—
R01	R03	R02	R07	R09	R101	R103	R102	R107	

112

012

92

82

72

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21

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42

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The diagram shows a 4-bit shift register represented by a horizontal rectangle divided into four cells. On the left, there are two input buses labeled 'A' and 'B', each with a 2-bit width. On the right, there are two output buses labeled 'C' and 'D', each with a 2-bit width. Arrows indicate the flow of data from the inputs into the register and from the register to the outputs.

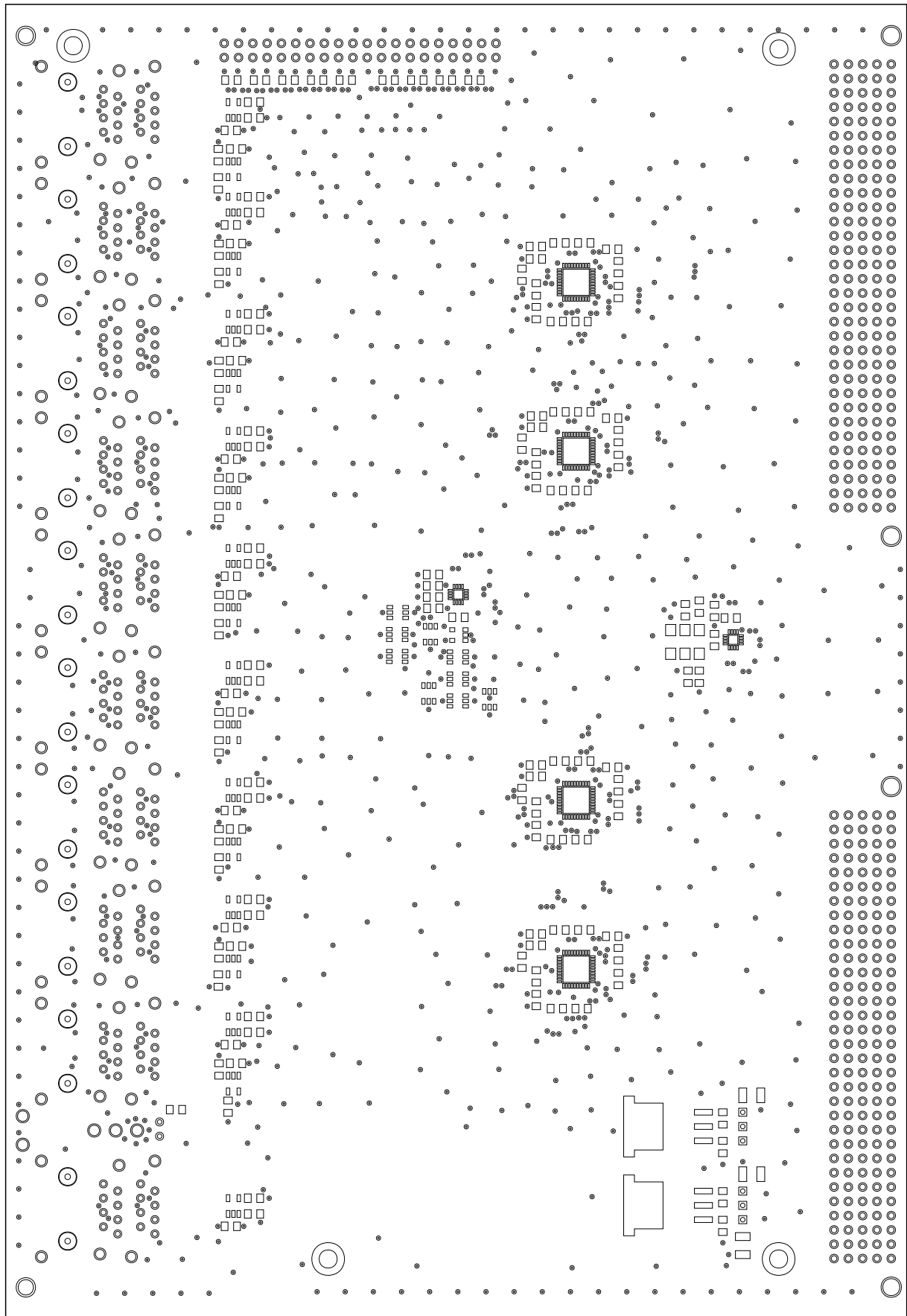
[illegible]

Σ	A	B	C	D	Σ
35					

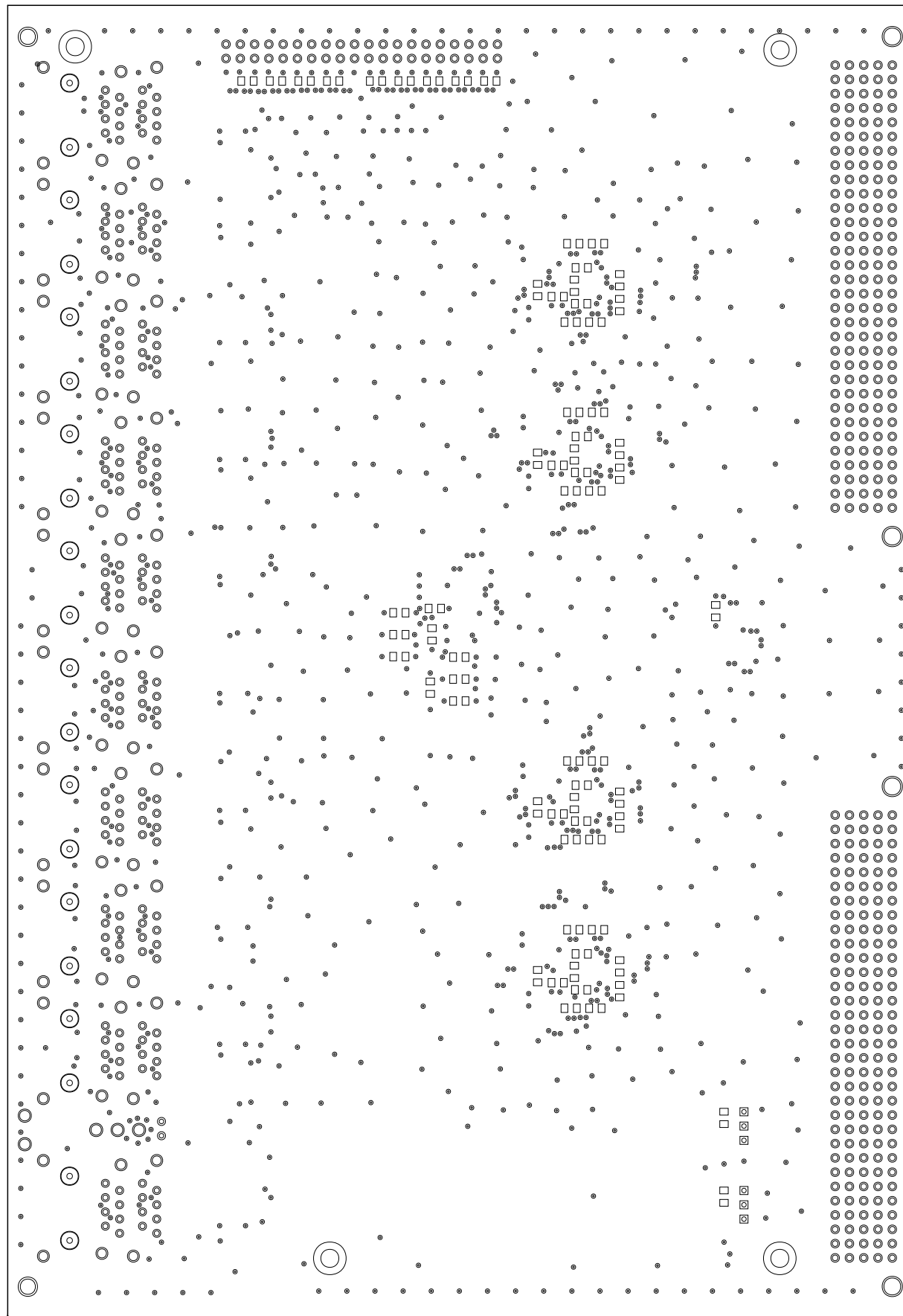
Σ	A	B	C	D
Σ	15			

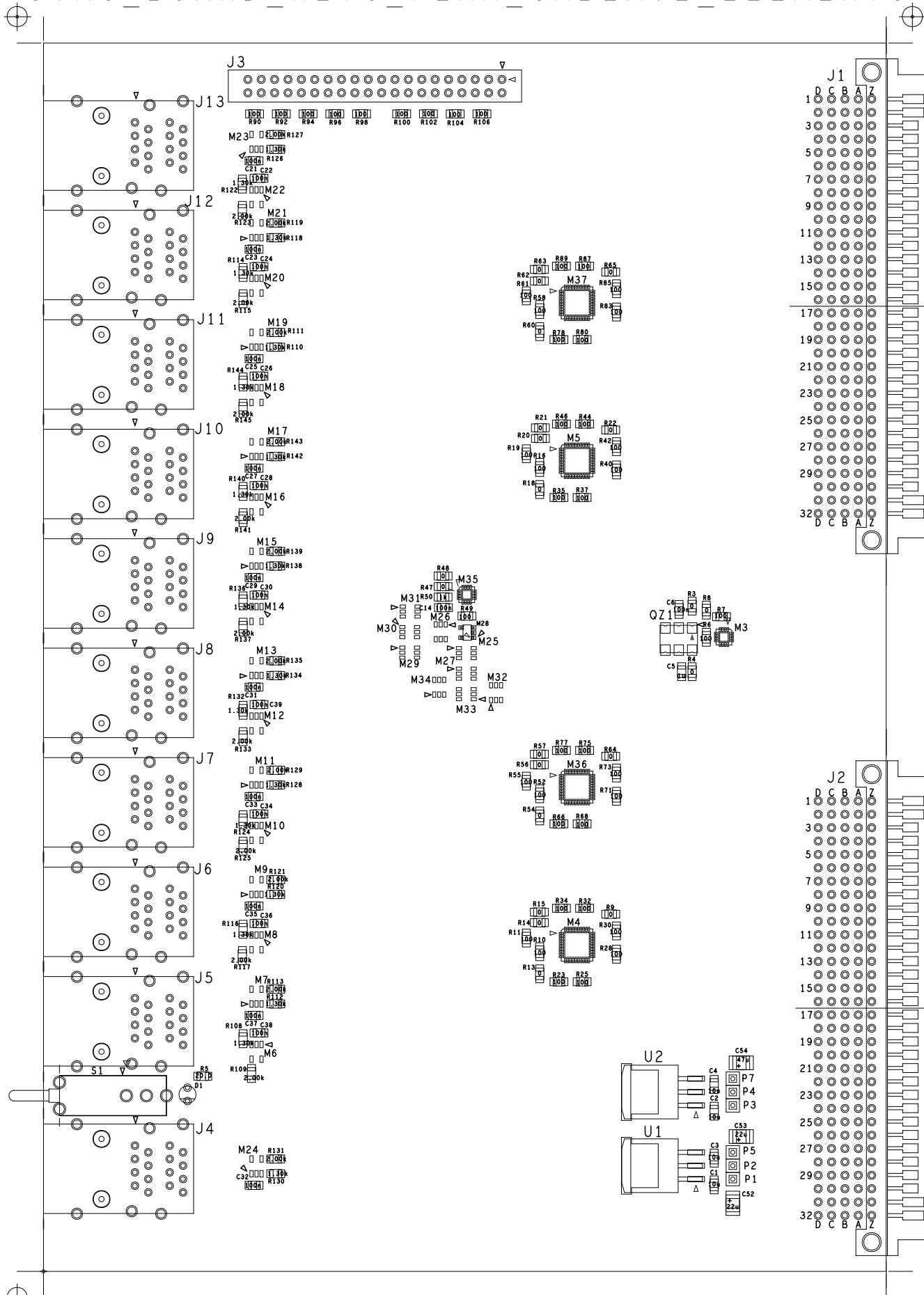
Δ	A	B	C	D	Σ
35					

SYNC_BOARD_REVC_VERNIS_EPARGNE_ELEMENTS



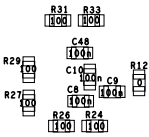
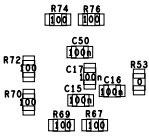
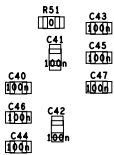
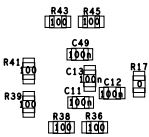
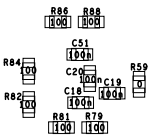
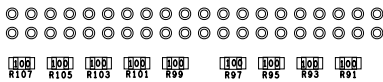
2 SYNC_BOARD_REV_C_VERNI2_EPARGNE_200DURE2



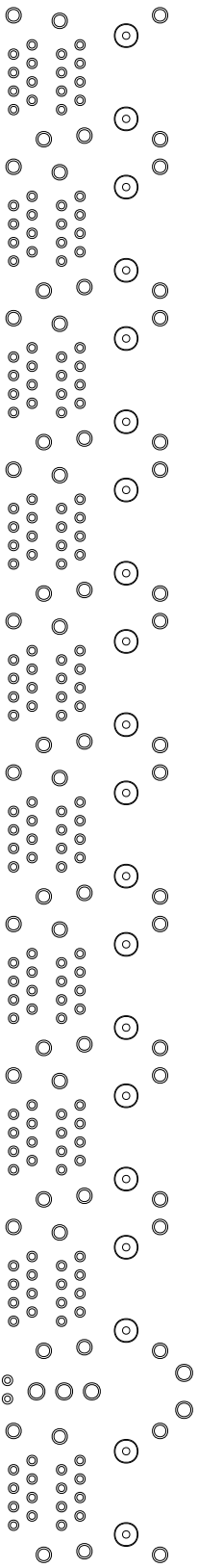


SYNC_BOARD_REVC_PLAN_CABLAGE_SOUDURES

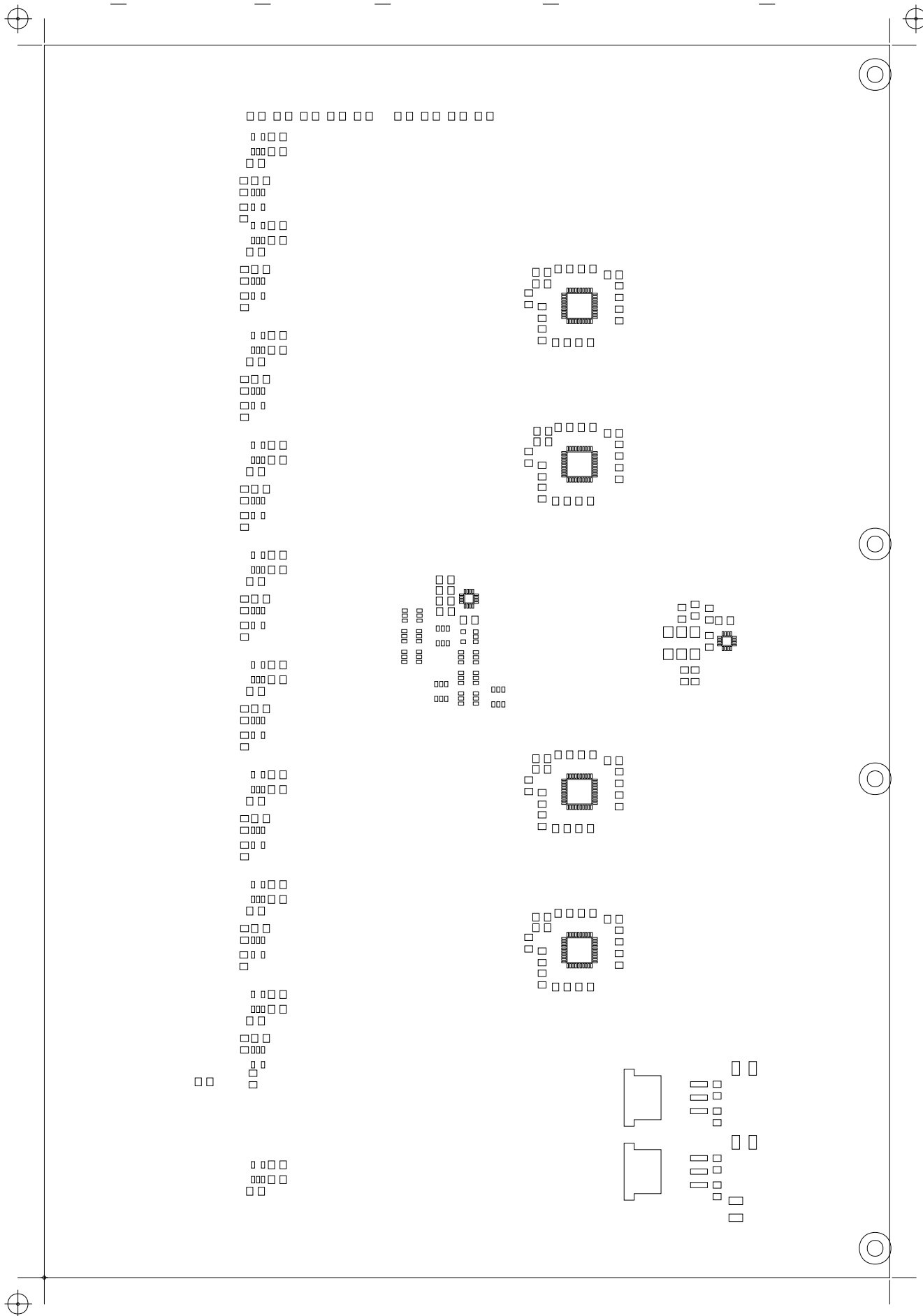
J1



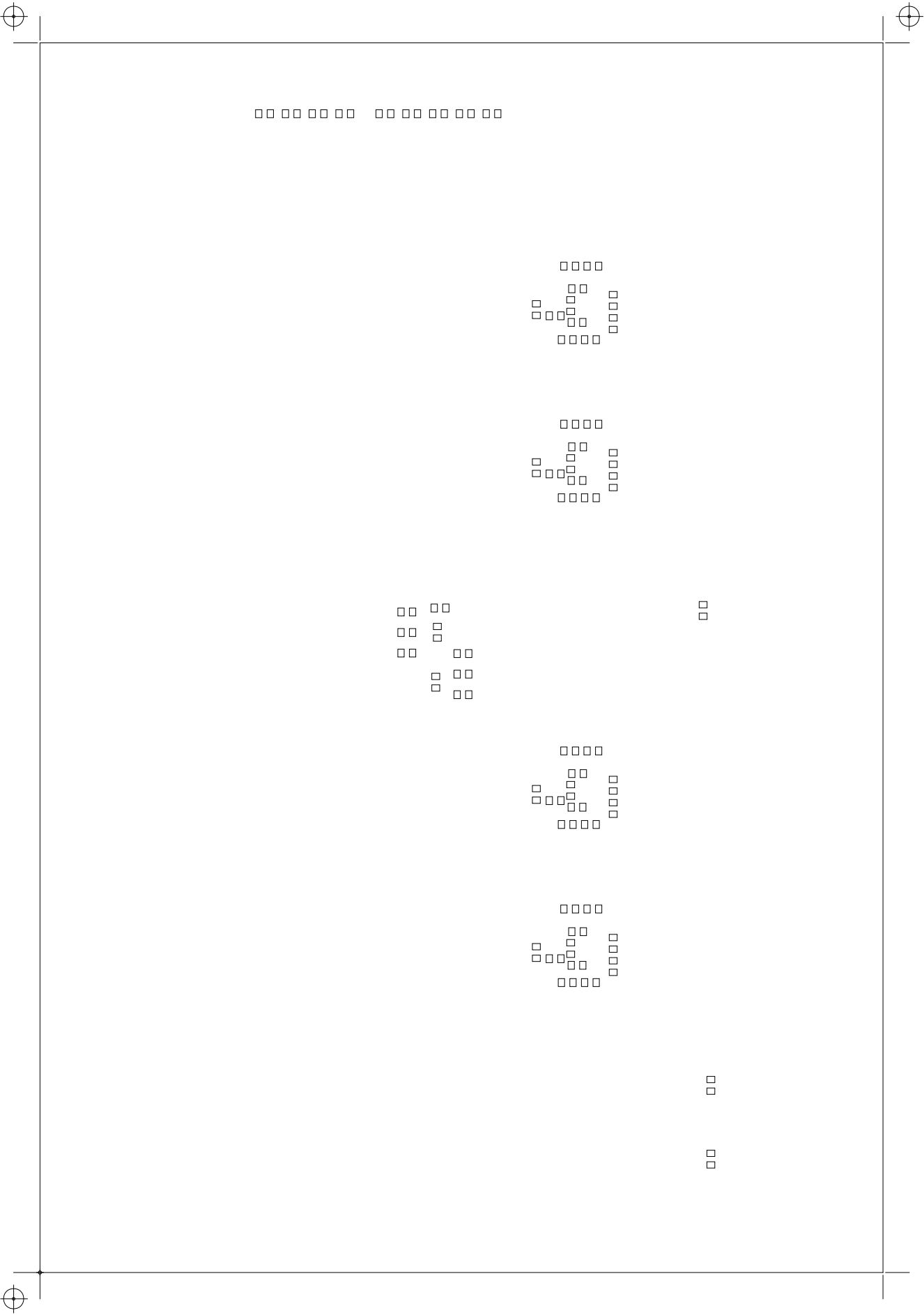
J2

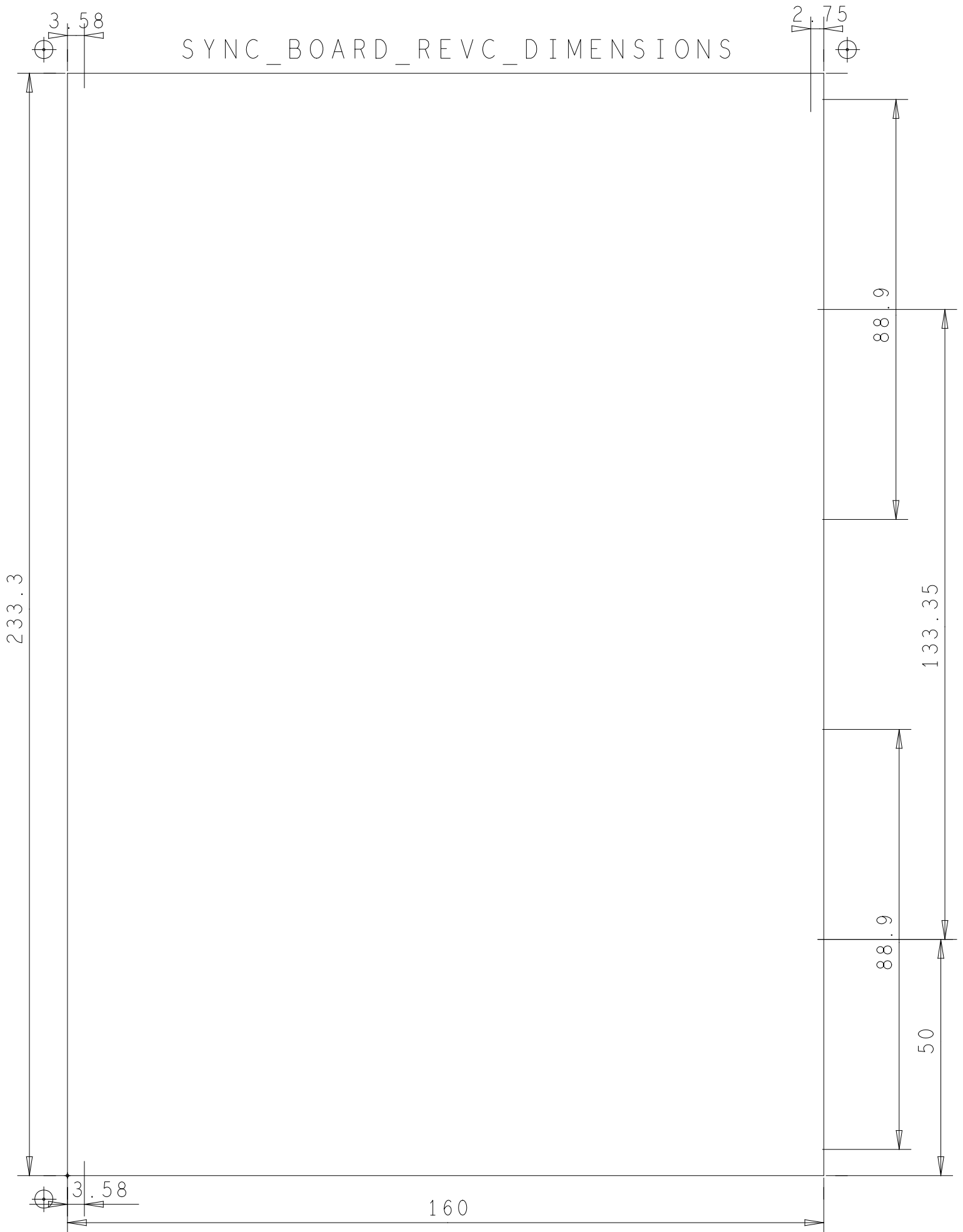


SYNC_BOARD_REVC_PLACES_SOUDURES_ELEMENTS

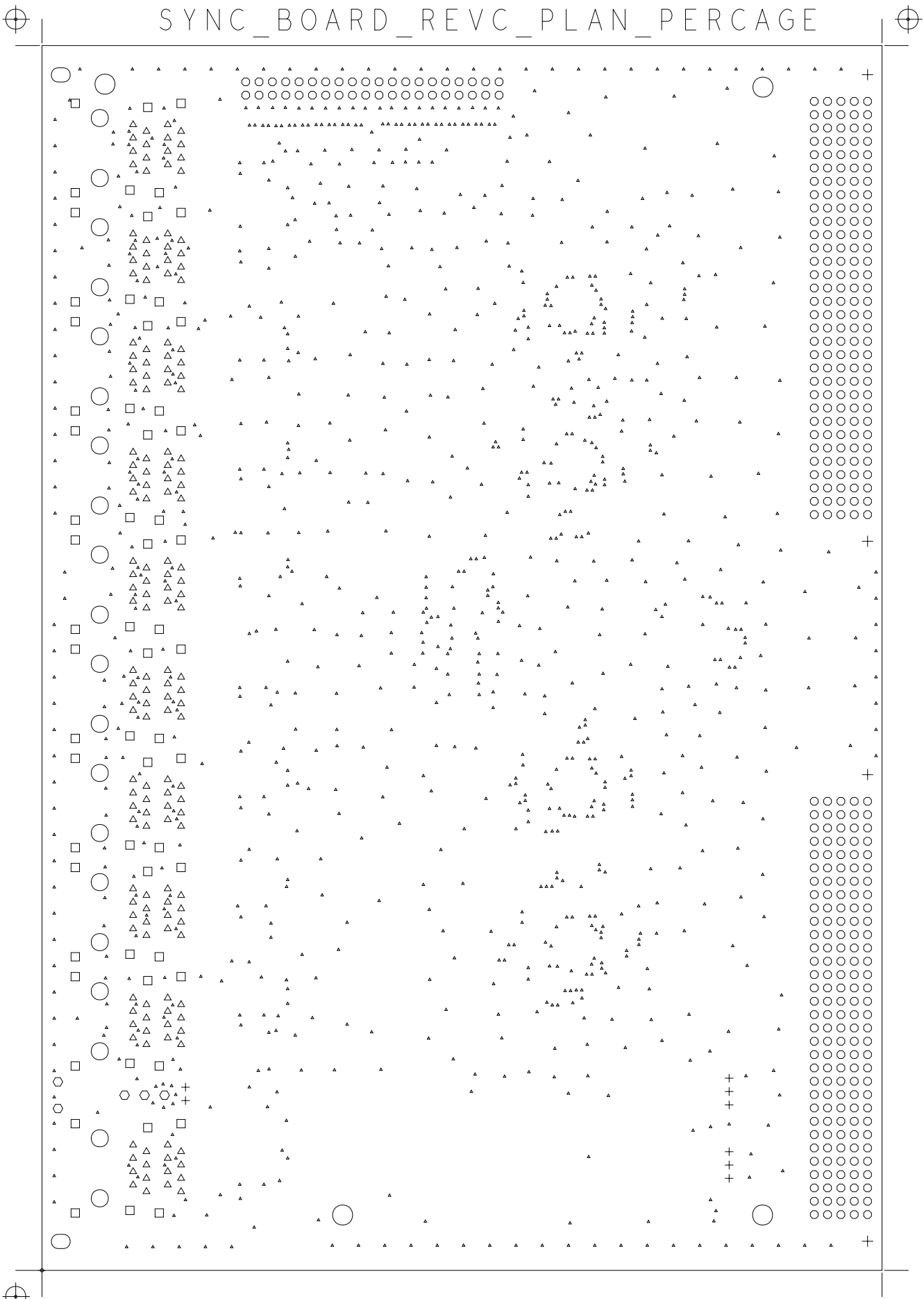


2 SYNC_BOARD_REVC_PLACES_2_SOUNDURES_2





SYNC_BOARD_REVC_PLAN_PERCAGE



DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	FINISHED_SIZE	PLATED	QTY
△	0.3	PLATED	1059
+	0.8	PLATED	8
△	0.9	PLATED	160
○	1.0	PLATED	360
□	1.6	PLATED	60
○	1.85	PLATED	5
○	2.7	PLATED	2
○	3.2	PLATED	4
+	3.0	NON-PLATED	4
○	3.25	NON-PLATED	20